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SECTION 1
Purpose and Main Features

PURPOSE

The 7804A card combines a buffered and fully expandable Z80A microprocessor with onboard memory (ROM and/or RAM), and a three-channel counter/timer with onboard interrupt and status polling system. The card is available in two options: the 7804A-0 with a 4.0 MHz CPU and the 7804A-1 which operates at 2.5 MHz.

An STD BUS system using the 7804A card can be expanded to the full Z80 memory and I/O capability. The card includes four 28-pin sockets for onboard memory, conforming to the JEDEC 28-pin standard. The 7804A STD BUS interface can be disabled for DMA and multiprocessor application with full external access to onboard devices.

The counter/timer provides three 16-bit counter/timer channels which are configured independently by the program. Each channel is suitable for frequency/event counting from DC to 2.5 MHz, pulse marker or squarewave generation, time interval measurements, one-shot simulation, and repetitive event generation.

FEATURES

- Z80A processor
- Crystal controlled 250 ns clock (7804A-0) or 400 ns clock (7804A-1)
- Up to 32K bytes of onboard ROM (2764) capacity or any combination of JEDEC 28-pin compatible ROM or RAM
- Three independent 16-bit counter/timer channels with six operating modes each
- Onboard counter/timer interrupt latches and masks
- Provision for external clock and gate signals to counters
- DMA capability
- Power-on and pushbutton reset
- Three-state address, data, and control bus
- Provisions for bootstrap operation
- Dynamic RAM refresh control
- Single +5V operation

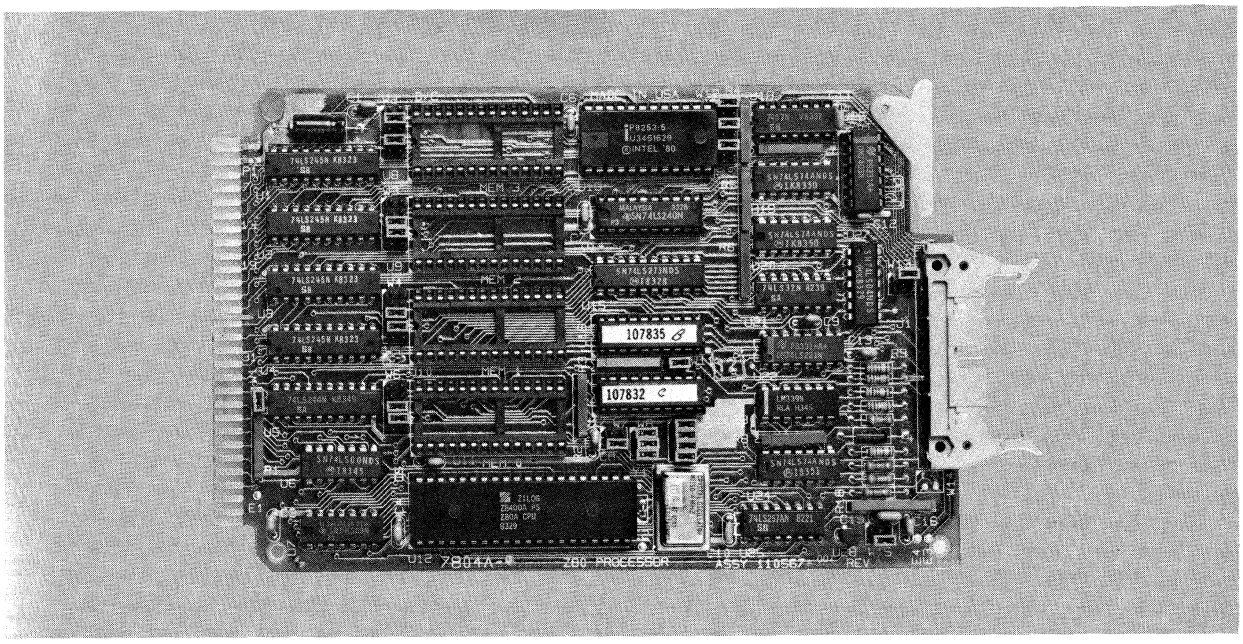
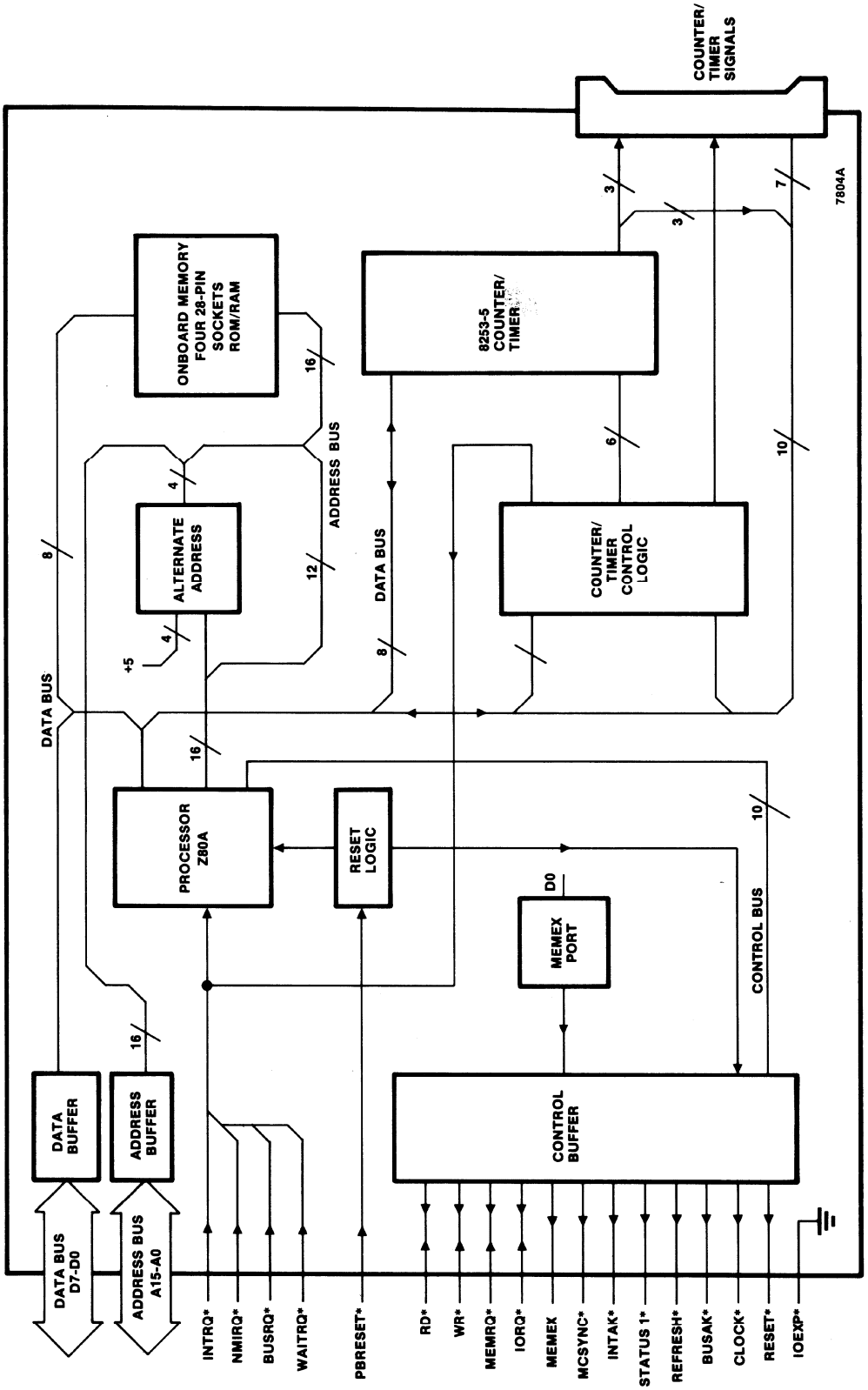


Figure 1-1. 7804A Z80A Processor Counter/Timer Card



*Low-Level Active Logic

Figure 1-2. Block Diagram of 7804A Processor Counter/Card

SECTION 2
Installation and Specifications

INTRODUCTION

This section explains the functions and options of the 7804A card to consider before installing the card in a system. It also includes the card's specifications.

The 7804A card can be used by itself in an STD BUS card rack, or as part of an STD BUS system. By itself, the card provides up to 32K of memory. A connector at the card ejector end of the 7804A includes the interface for the 7804A counter/timer plus one input line and one output line. In an STD BUS system, you can use the 7804A with STD BUS memory cards, I/O cards, and peripheral cards.

> **NOTE**
>
> To prevent possible damage to your STD BUS system, make sure that power is off before inserting a card in the card rack, or before removing a card from the card rack.

At installation, insert the 7804A in any slot in the card rack, with the card ejector positioned towards the top of the card rack (see figure 2-1).

To access the 7804A, install it in either end of an open-ended card rack, or use a Pro-Log 7901 card extender. Plug the 7901 into any slot in the card rack and plug the 7804A into the 7901.

The 7804A's interface connector is a latching 26-pin connector with alternating signal and ground lines for use with a connector twisted-pair cable (e.g., Pro-Log's RC704), or a 26-conductor cable with mating connector. Part numbers for the mating connectors are listed in figure 2-2.

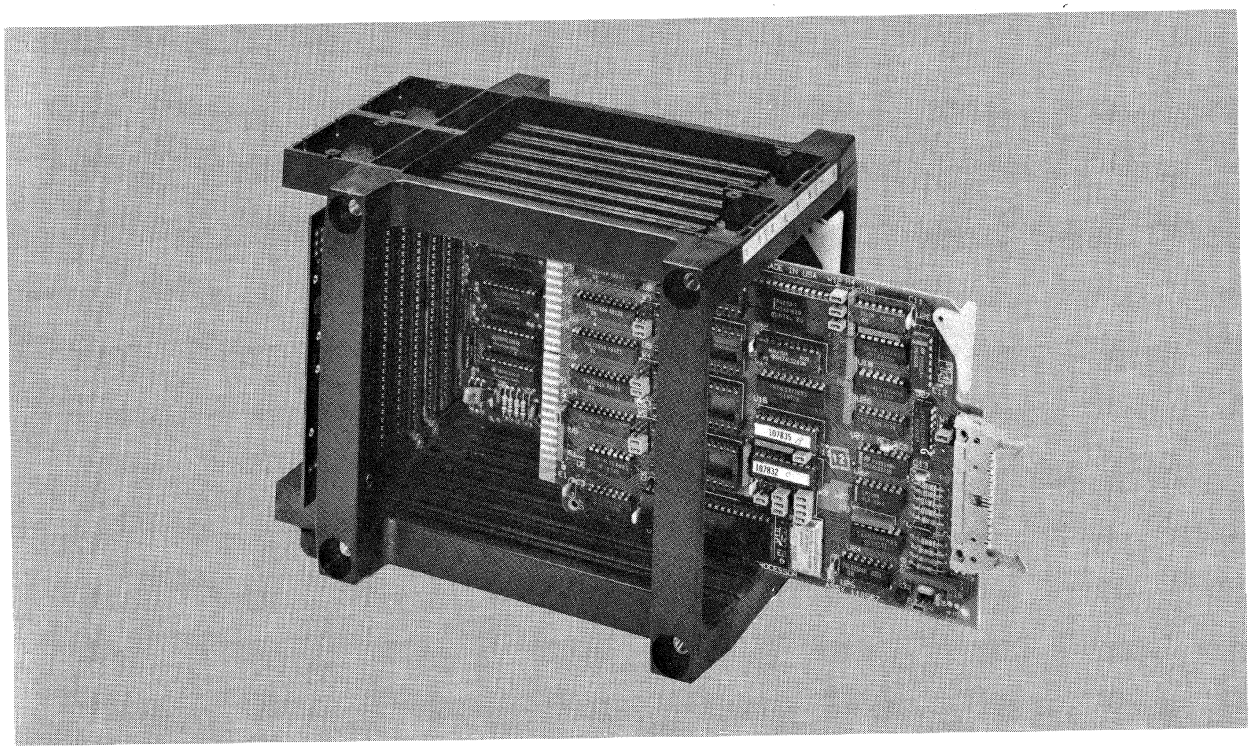


Figure 2-1. Installation of 7804A Card in STD BUS Card Rack

ALTERNATIVES TO SOLDERED WIRE JUMPERS

The 7804A has several optional functions that are selectable by wire jumpers. To remove and replace these jumpers, cut each jumper in half, and desolder and remove each half individually. This procedure prevents damage to circuit traces.

If occasional or frequent changes in address mapping jumpers are anticipated, remove the wire jumpers and substitute permanent 0.025-in (0.64 mm) square posts. The posts can be connected by slip-on, slip-off connectors. Recommended headers and connectors are listed in figure 2-2. The location of the 7804A's jumpers and other main components is shown in figure 2-3.

PART	MANUFACTURER PART NUMBER	
	ELCO CORP.	BERG ELECTRONICS
2-PIN HEADER	00 8261 02 32 00 852	65611-102
4-PIN HEADER	00 8261 04 32 00 852	65611-104
6-PIN HEADER	00 8261 06 32 00 852	65611-106
8-PIN HEADER	00 8261 08 32 00 852	65611-108
CONNECTOR	00 8261 02 42 00 870	

Figure 2-2. Recommended Headers and Connectors (7804A)

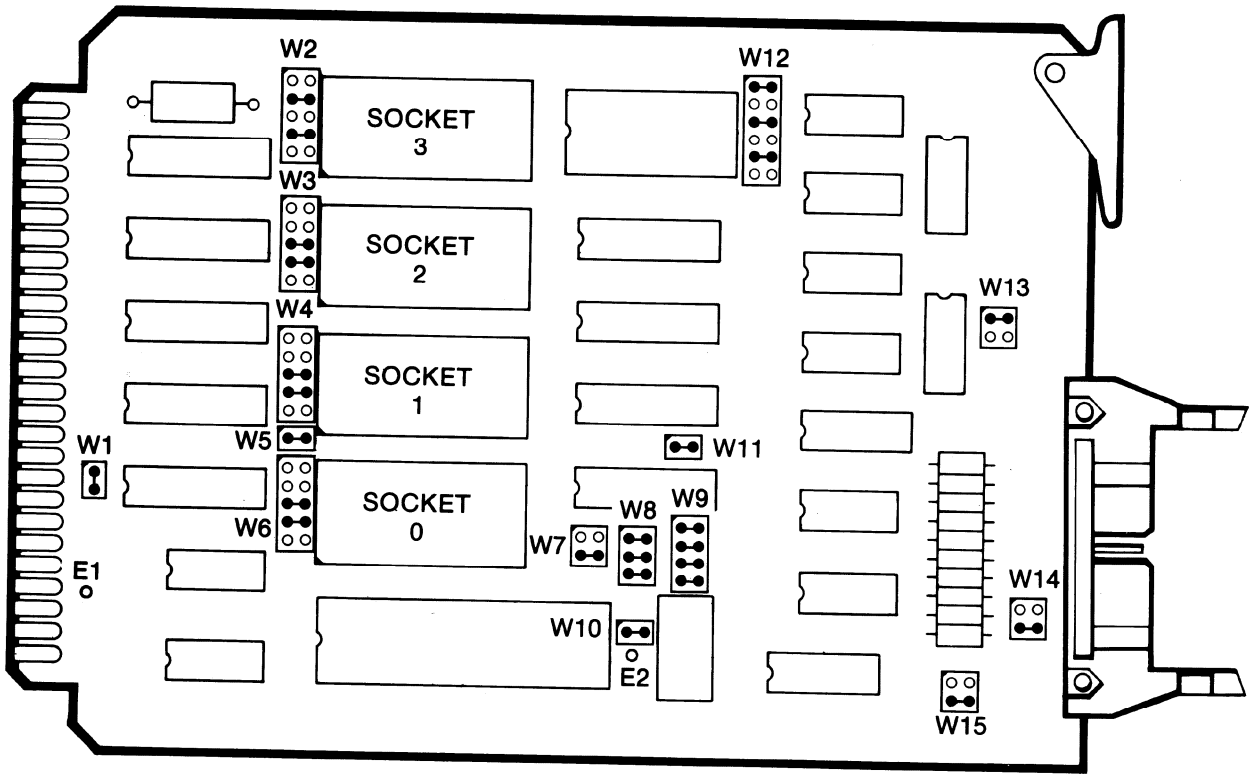


Figure 2-3. Jumper Location (7804A)

MEMORY DECODER

The four memory sockets of the 7804A accept any combination of 2K, 4K, or 8K EPROMs/ROMs and RAMs that conform to the specifications described in this section under "Memory Type." It is also possible to use 2K EPROMs. However, at this time no 2K EPROMs have the required 250 ns access times. If 2K EPROMs with the required speed become available in the future, they can be used. Also, pin-compatible PROMs and ROMs that have the required speed can be used in place of any of the EPROMs.

The combination of memory types and the address range each socket occupies are controlled by the memory decoder, which contains eight optional combinations selected by wire jumpers W8-1 & -2, & W8-3 & -4, and W8-5 & -6. See figure 2-3 for the location of these jumpers. The eight combinations and the method of selecting them are shown in figure 2-4.

Respective 64K memory maps, showing the address field occupied by each socket for each option, are given in figures 2-5 through 2-12.

The memory decoder is a PROM. If you require other combinations of memory types or other address mapping, replace the PROM with one containing your own program. The options contained in the memory decoder as shipped should suffice for most user applications. If other options are required, the writing of the program and the programming of the PROM are the responsibility of the user.

OPTION	MEMEX	JUMPERS W8			MEMORY SIZES	TOTAL MEMORY	ADDRESS RANGE	COMMENTS
		1&2	3&4	5&6				
1	Low				3-4K, 1-2K	14K	0000-37FF	Standard configuration; sockets come set up for three 4K EPROMs and one 2K RAM.
2	Low	x			4-2K	8K	0000-1FFF	
3	Low		x		4-4K	16K	0000-3FFF	
4	Low	x	x		4-8K	32K	0000-7FFF	
5	Low			x	1-4K, 3-2K	10K	0000-27FF	
6	Low	x		x	3-8K, 1-2K	26K	0000-67FF	
7	Low		x	x	1-4K	4K	F000-FFFF	For use with bootstrap function; see "Bootstrap" subsection.
8	High	x	x	x	1-4K	4K	0000-0FFF	A second form of bootstrap; requires use of MEMEX line.

x = Jumper removed.

Figure 2-4. Memory Decoder Options (7804A)

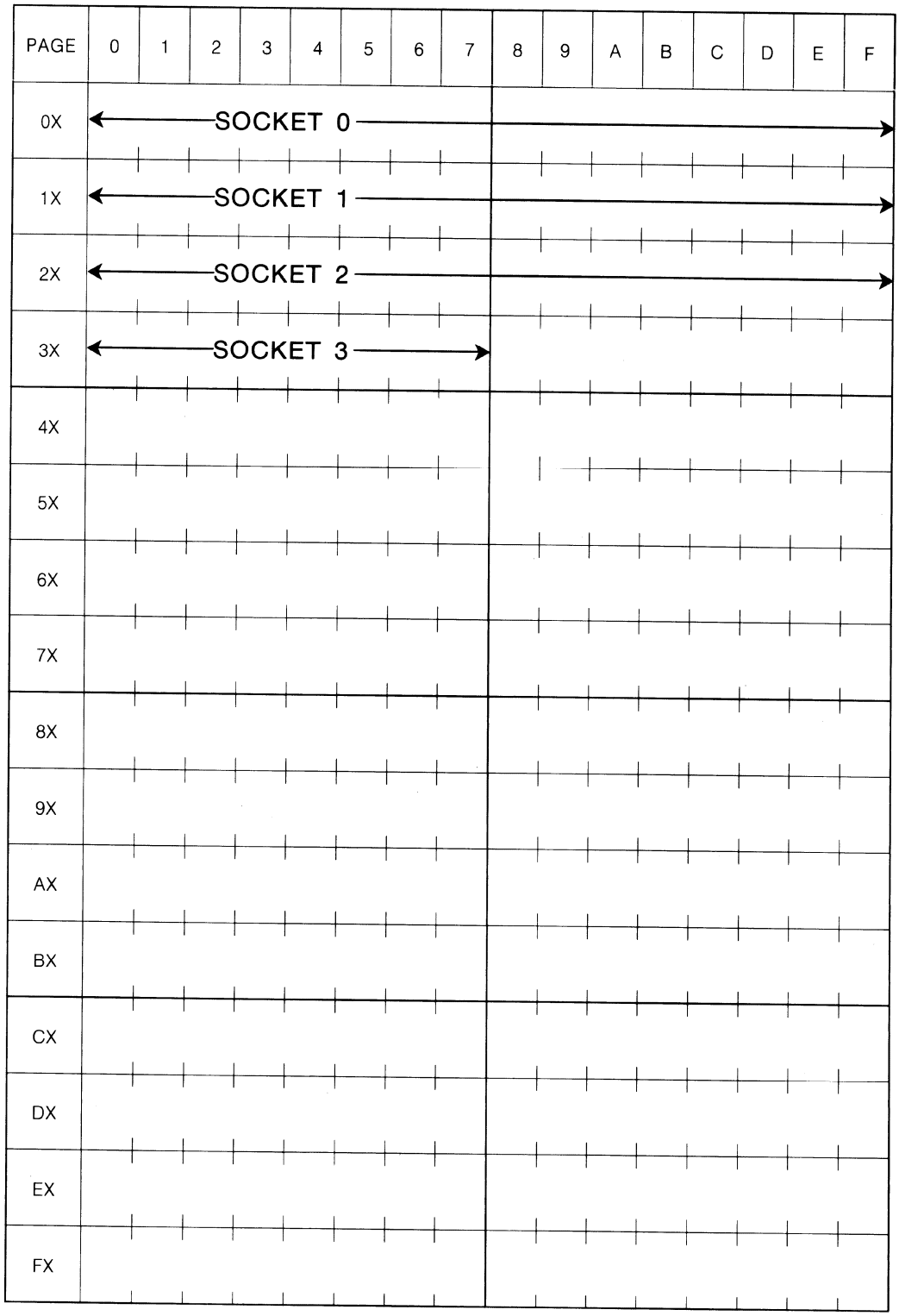


Figure 2-5. Memory Decoder Option 1 (7804A)

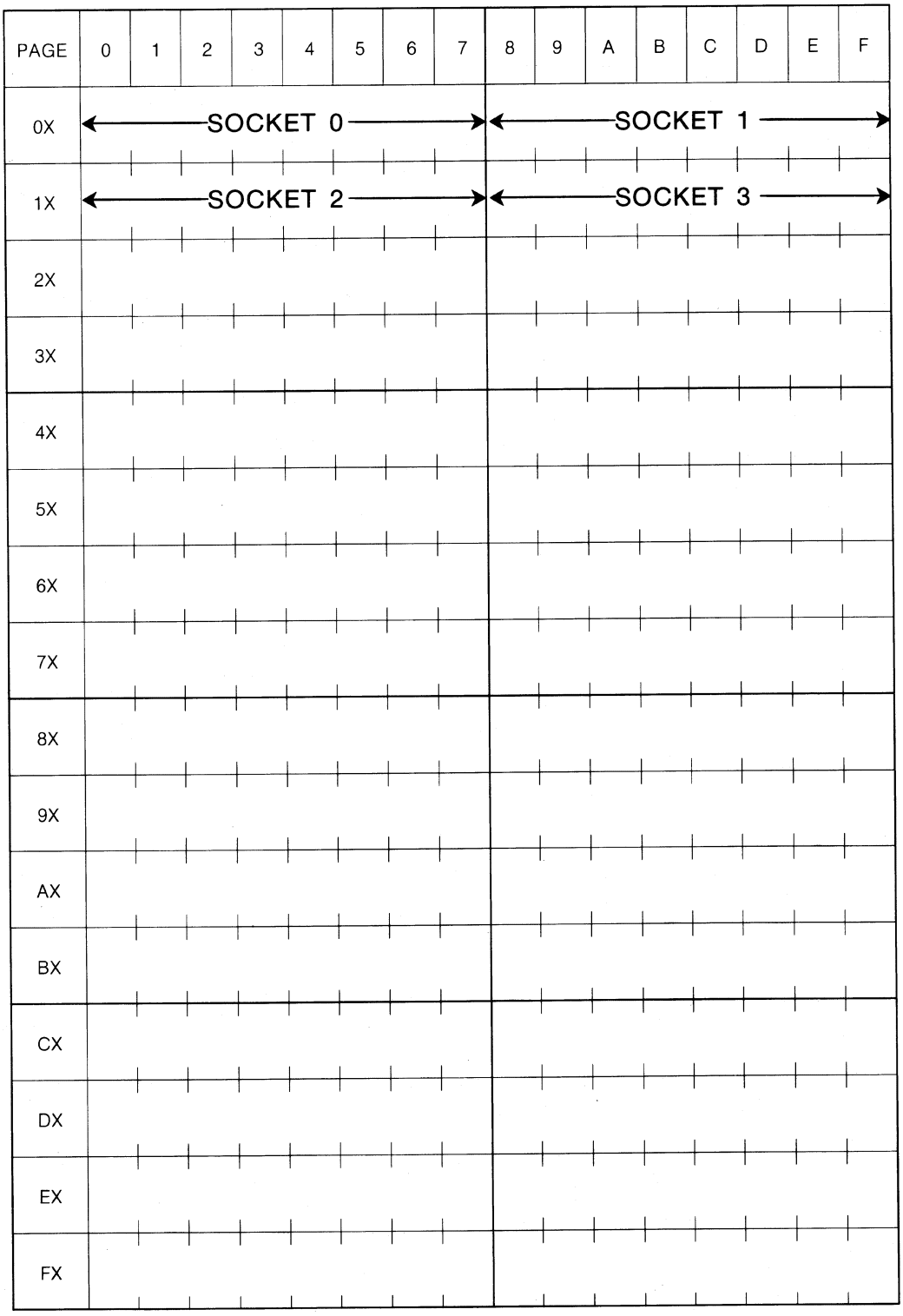


Figure 2-6. Memory Decoder Option 2 (7804A)

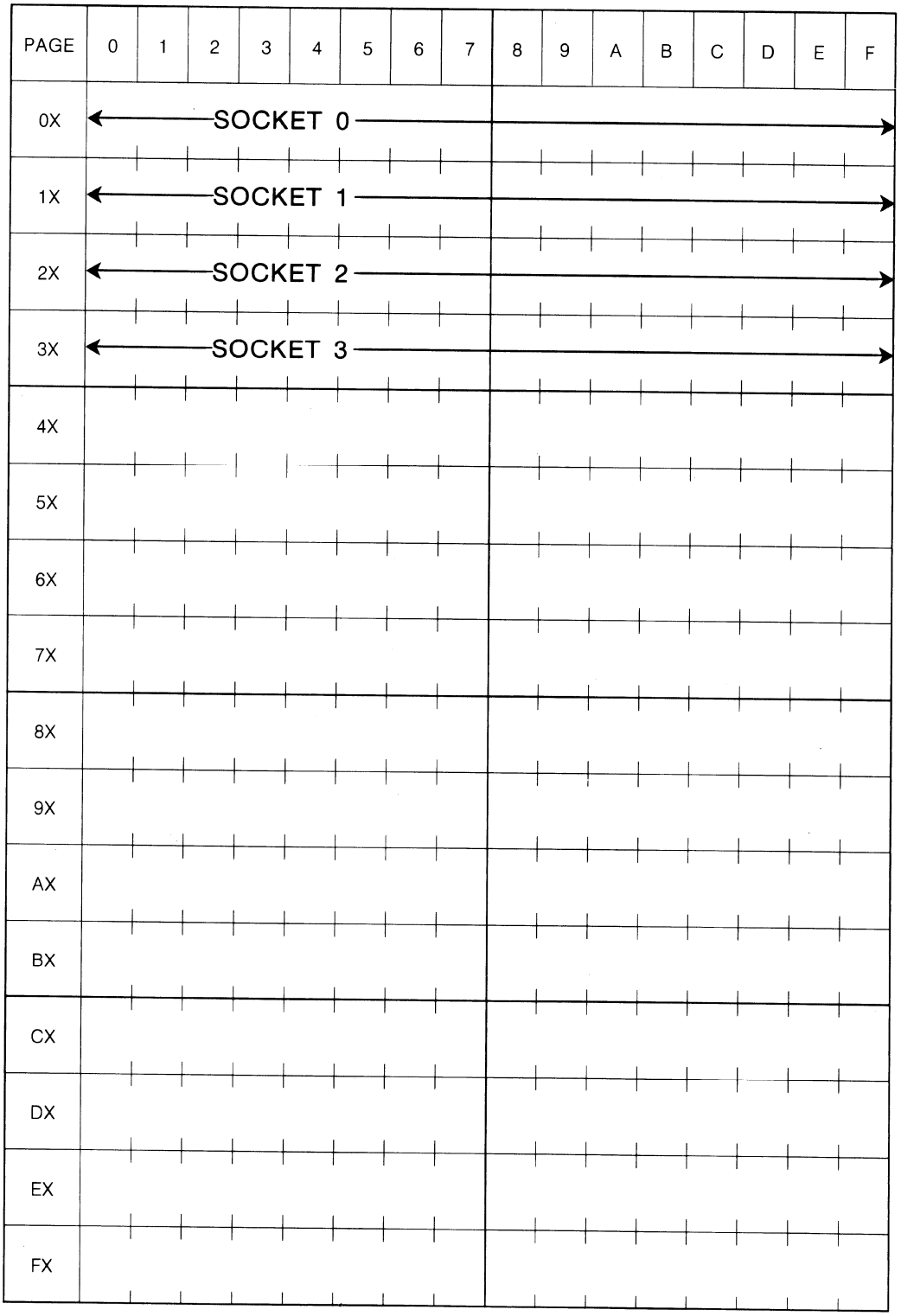


Figure 2-7. Memory Decoder Option 3 (7804A)

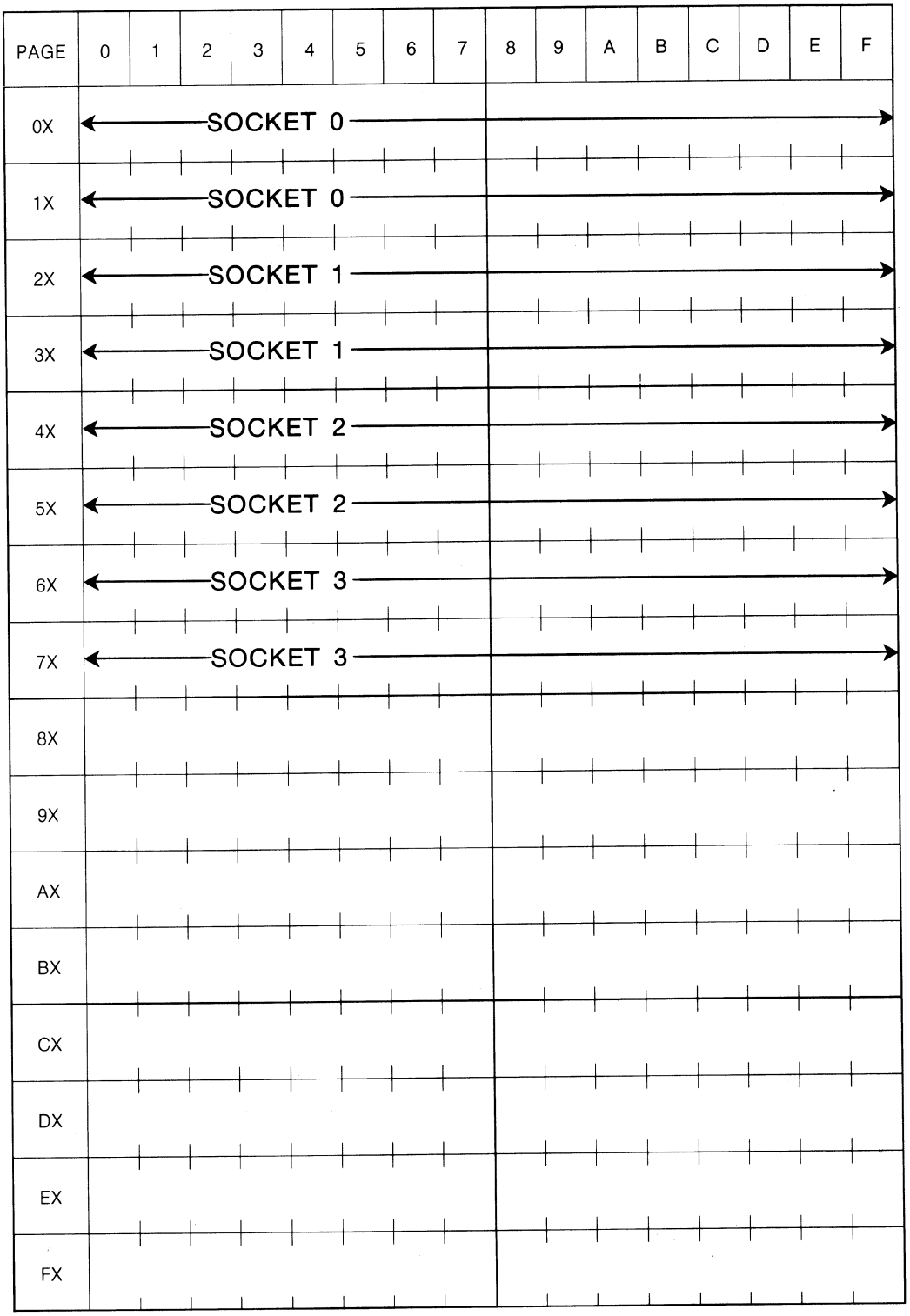


Figure 2-8. Memory Decoder Option 4 (7804A)

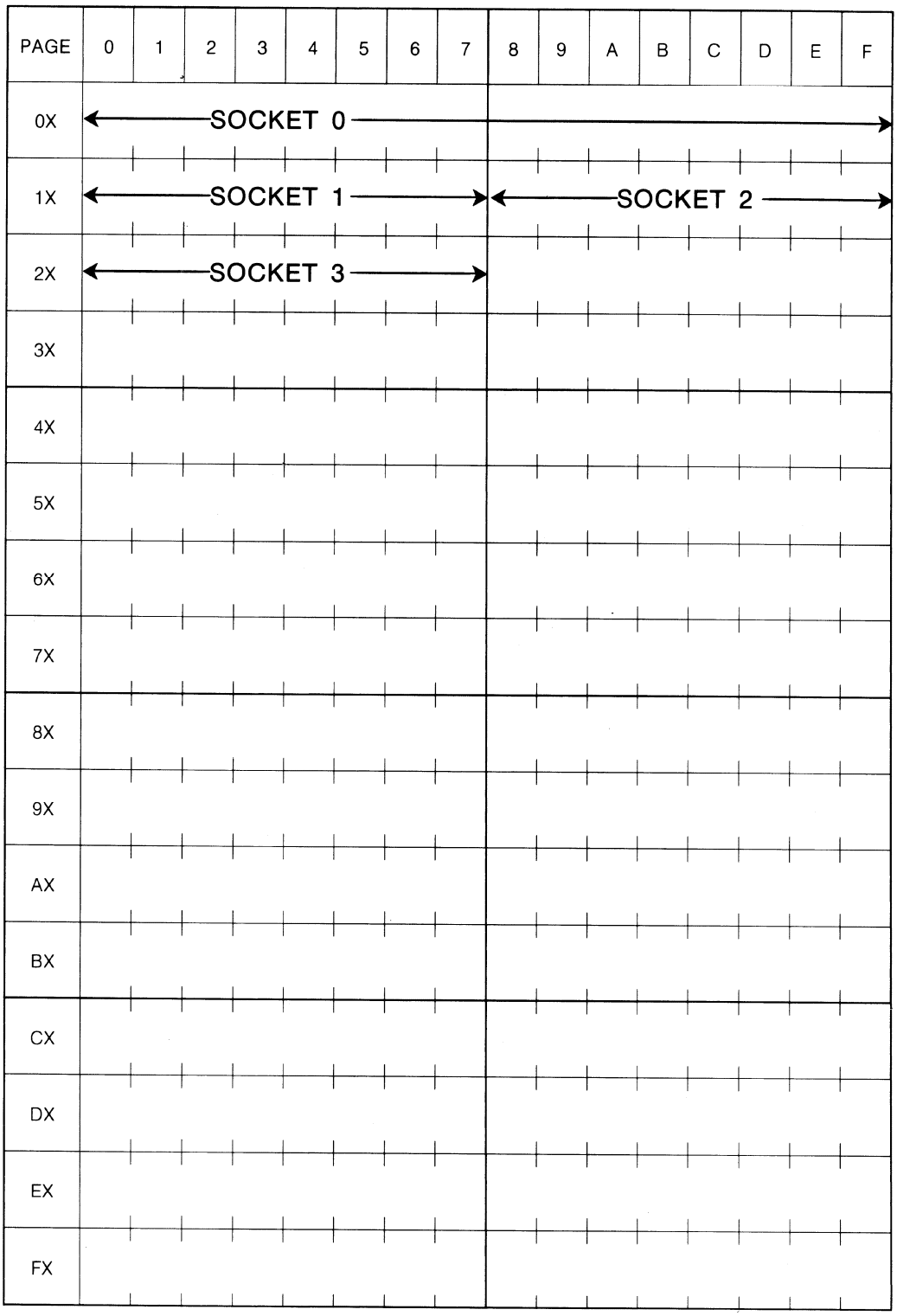


Figure 2-9. Memory Decoder Option 5 (7804A)

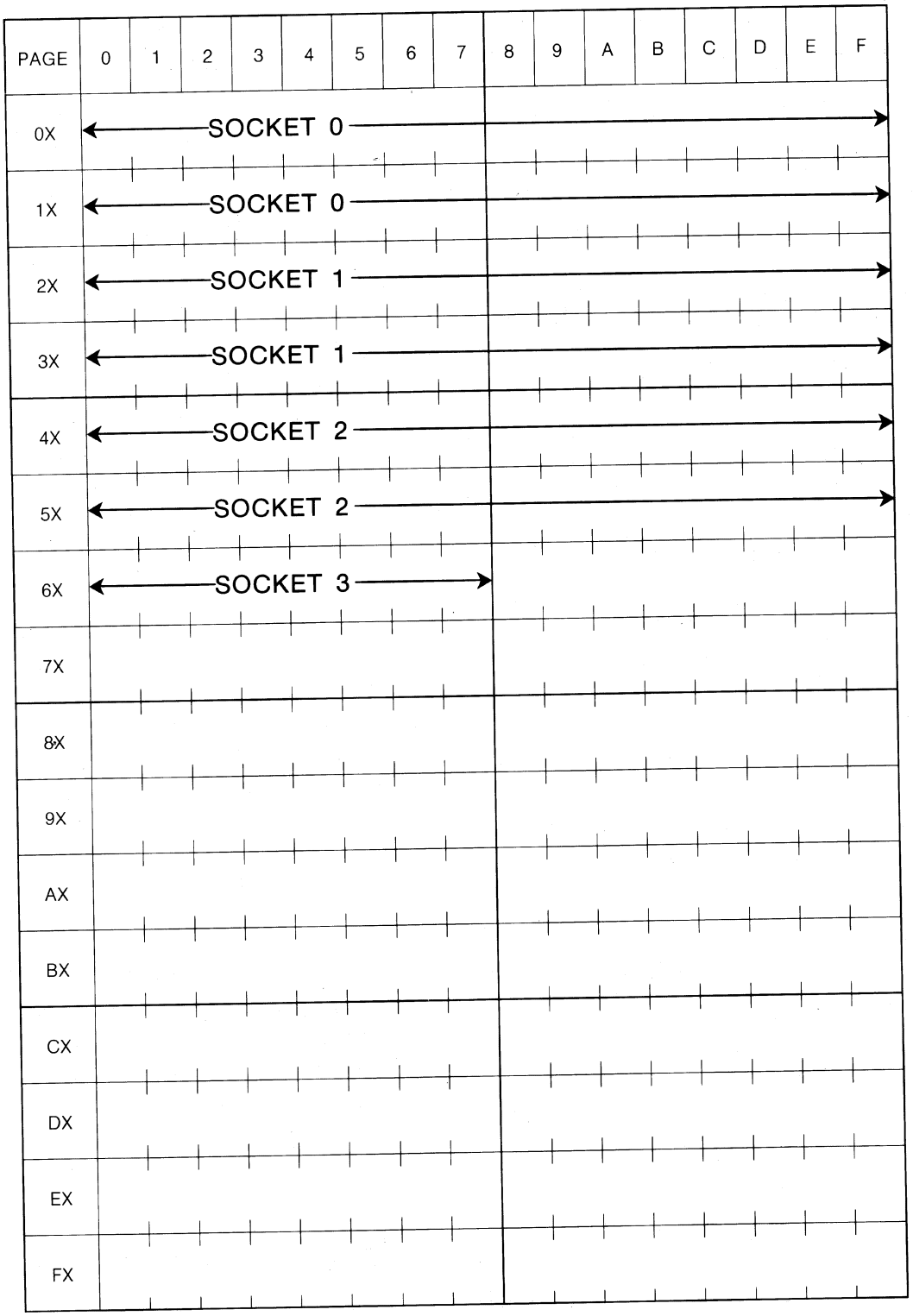


Figure 2-10. Memory Decoder Option 6 (7804A)

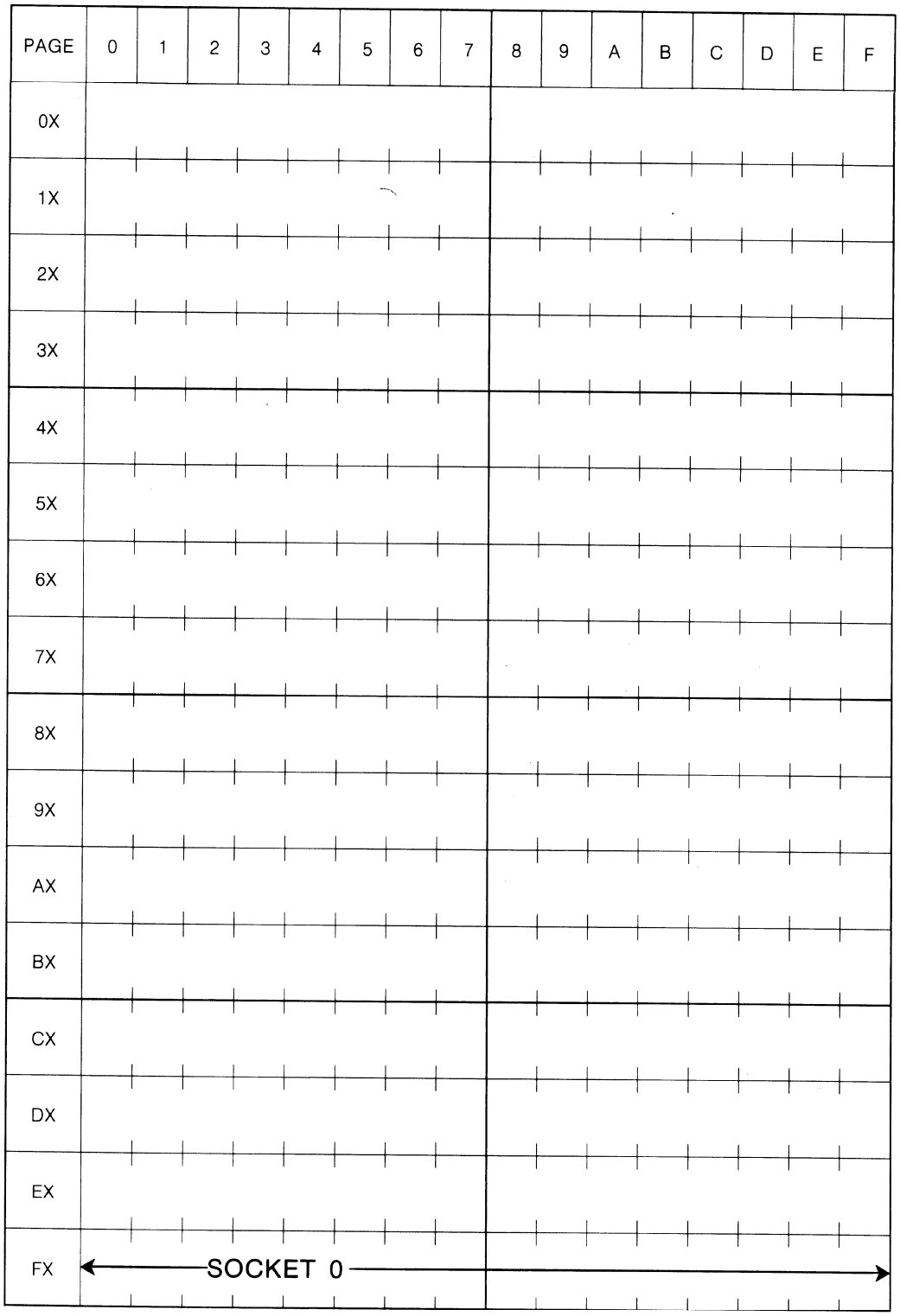


Figure 2-11. Memory Decoder Option 7 (7804A)

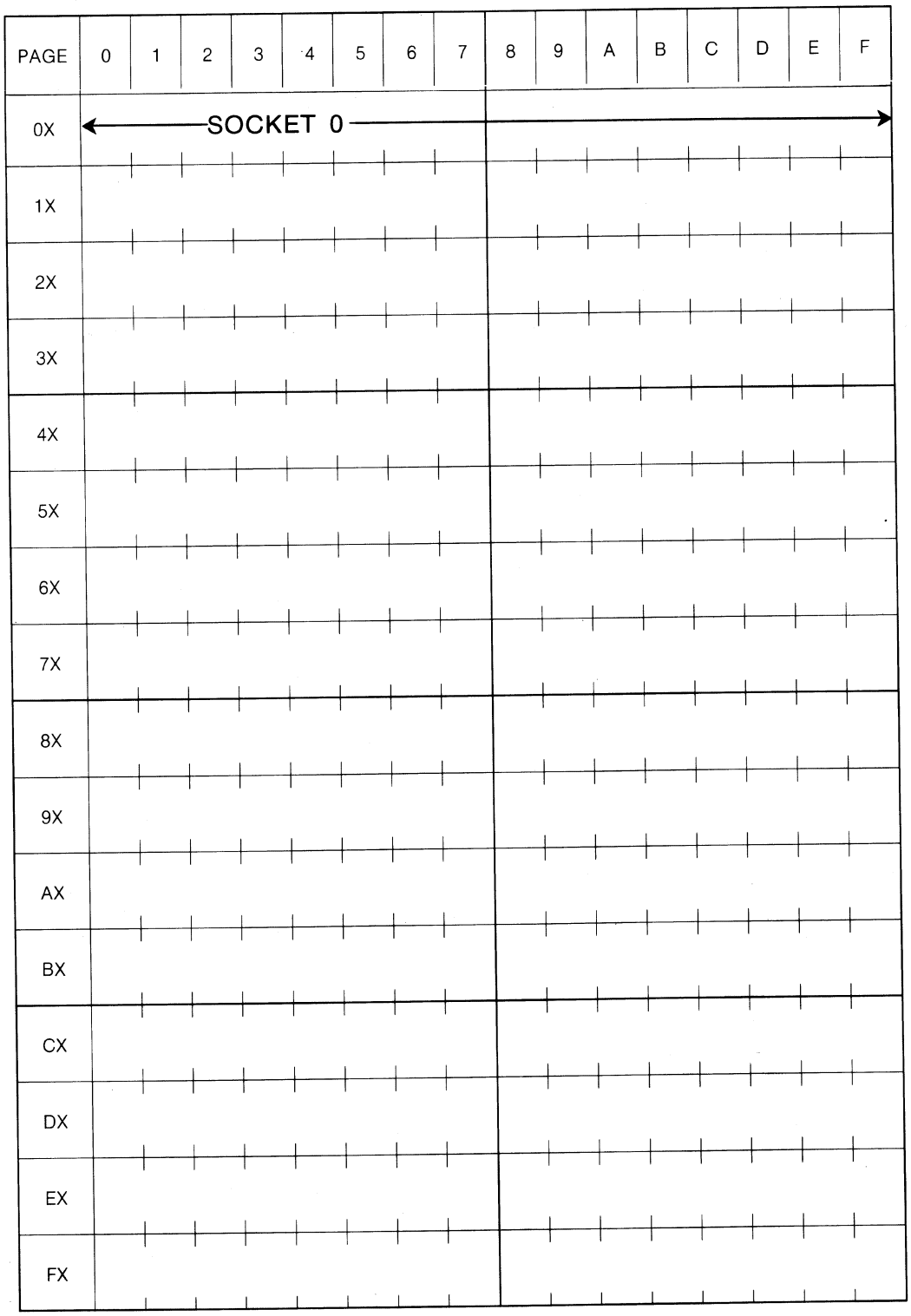


Figure 2-12. Memory Decoder Option 8 (7804A)

MEMORY TYPE

The 7804A can use three different kinds of memory: 2K RAMs, 4K EPROMs/ROMs, and 8K EPROMs/ROMs or RAMs. It can also use 2K EPROMs. However, as mentioned before, no 2K EPROMs are now available with the required 250 ns access time. If 2K EPROMs with the required speed become availabe in the future, they can be used. Also, pin-compatible PROMs and ROMs that have the required speed can be used in place of any of the EPROMs. The 7804A's four memory sockets accept memory components compatible with the JEDEC 28-pin standard pinout. Each socket can be individually configured, using wire jumpers, for any one of the four memory types.

Once you have chosen the memory combination that suits your needs (as discussed in the "Memory Decoder" subsection), configure the sockets accordingly. Figure 2-13 shows where to place the memory socket jumper for each kind of memory. These jumpers are shown in figure 2-3. Jumpers W6, W4, W3, and W2 correspond to sockets 0, 1, 2, and 3, respectively.

Figure 2-14 lists the components recommended for use on the 7804A card. To use other memory components, they must be compatible with the 7804A's socket configurations. Also, check for any special requirements they might have to be sure that their access times are no greater than 250 ns.

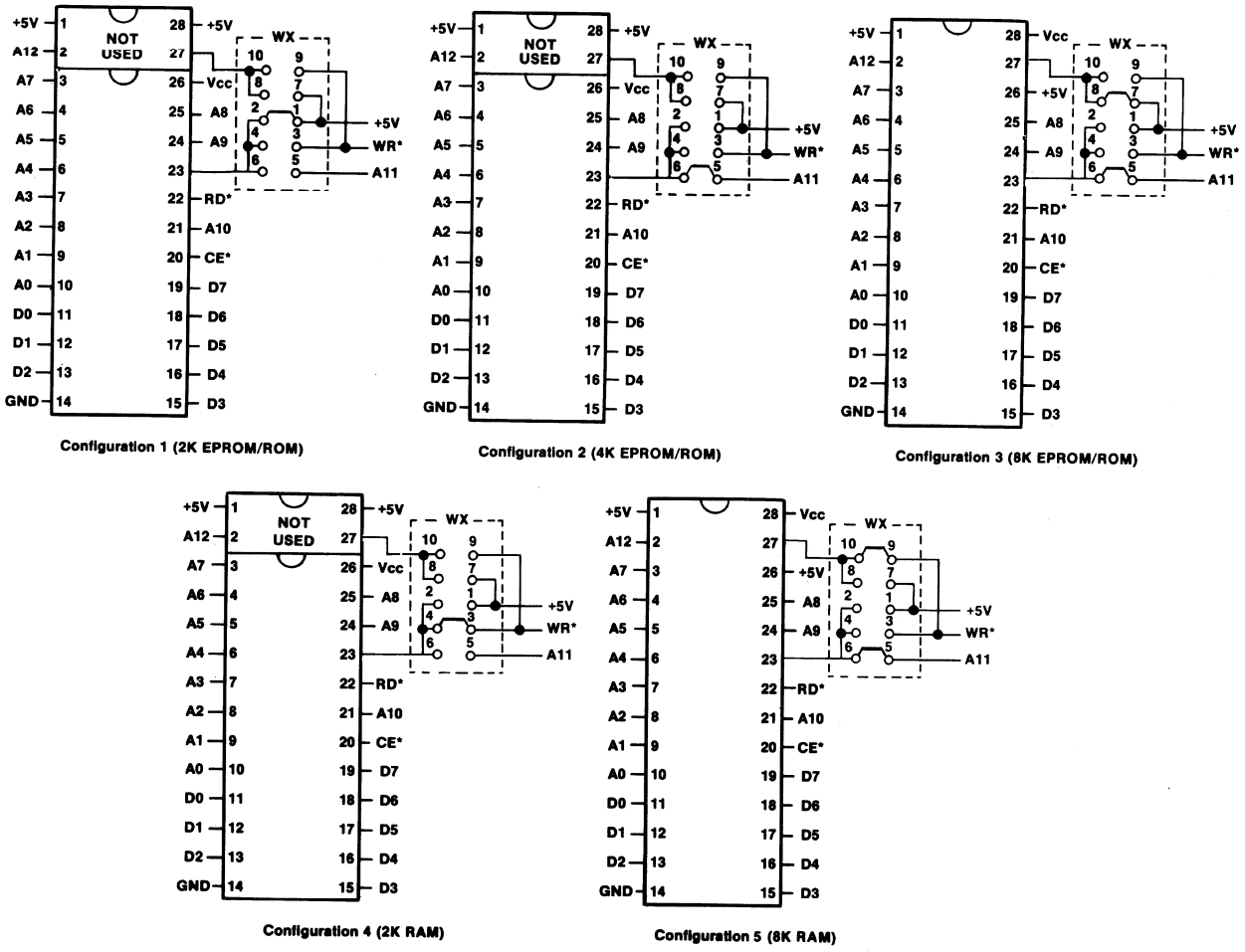


Figure 2-13. Socket Configurations (7804A)

Type	Part #	Manufacturer
2K RAM	M58725P	Mitsubishi
2K RAM	MSM5128	OKI
2K RAM	TMM2016P	Toshiba
2K ROM	**2716	Intel
4K EPROM	2732A	Intel
8K EPROM	2764	Intel
8K RAM	HM6264p	Hitachi
8K RAM	*MSM5165	OKI

*Not available for testing
**2716 access time must be less than 250 ns (see text)

Figure 2-14. Tested Memory Components (7804A)

UNUSED SOCKETS

Along with the different memory types and configurations open to MEMEX, the 7804A's unused sockets can be disabled as a further tailoring of the onboard memory to suit your application. The disable jumpers are W9-7 & -8 through W9-1 & -2 which correspond to sockets 0 through 3 respectively. Their locations are shown in figure 2-3.

When one or more of these jumpers is removed over the address range that would be occupied by the corresponding socket, the 7804A is free to access memory on other cards in the system rather than the onboard memory. The address range that would be occupied by the socket is specified by the memory decoder option chosen. This means that no memory space is wasted by unused sockets. Also, onboard memory can occupy as little as 2K of memory space. If all four jumpers are removed, the onboard memory is completely disabled. Alternately, if jumper W7 (described in the next subsection) is removed, the onboard memory is disabled.

NOTE

Options 7 & 8 for bootstrap applications use only socket 0. The other sockets occupy no memory space and their jumpers do not have to be removed to disable them.

NOTE

To avoid data bus contention, do not install memory components in unused sockets.

MEMEX FOR ONBOARD MEMORY

This subsection explains how the MEMEX signal affects the 7804A's onboard memory. For a detailed explanation of the signal, see section 3.

Jumper W7, shown in figure 2-3, controls how the MEMEX signal affects onboard memory. With jumper W7 in position 3-4, as it is when the 7804A is shipped, the onboard memory is not affected by MEMEX and is always ready to be accessed by the processor. With jumper W7 in position 1-2, the onboard memory can be accessed only when MEMEX is in the low state. When MEMEX is in the high state, onboard memory is disabled. Then memory on other cards in the system can be read from, or written to, in the address range otherwise occupied by the onboard memory. If jumper W7 is removed completely, onboard memory is permanently disabled.

NOTE

The exception to onboard memory being disabled in the high state is memory decoder option 8. This option requires MEMEX to be high for it to be enabled. Its memory mapping is described in the "Memory Decoder" subsection.

MEMEX JUMPER OPTIONS

The MEMEX line is controlled by an output port and, as shipped, the data latch is reset after power-up or after pushbutton reset. To invert the output, jumper W13 (shown in figure 2-3) can be removed from position 1-2 and installed in position 3-4.

Jumper W1 must be enabled (as it is when the card is shipped) if the 7804A is to be used to control MEMEX. If MEMEX is to be controlled by some other card in the system, remove jumper W1. If you remove this jumper, do not leave the signal floating.

Note that MEMEX can control onboard memory even if some other card in the system is controlling MEMEX.

BOOTSTRAP FUNCTION

The bootstrap function is required in applications where the processor starts reading memory at an address other than 0000 after power-up or after pushbutton reset. The 7804A has the option of starting at address F000.

To effect this function, remove jumper W15 (shown in figure 2-3) from position 3-4 and place it in position 1-2. This sets the four most significant address lines in the logic-one state after power-up or after pushbutton reset.

When using the bootstrap option, a ROM containing the user's start-up program should reside at address F000. This ROM can be either on the 7804A or on some other card in the system. If onboard memory sockets are to serve this purpose, memory decoder option 7 should be used. This option maps memory socket 0 to address range F000-FFFF; no other memory sockets are utilized and they occupy no memory space. See "Memory Decoder" subsection for an explanation of option 7.

Also, when using the bootstrap option, socket 0 should be configured to accept a 4K EPROM/ROM, as it is when the card is shipped. Socket configurations are explained in the "Memory Type" subsection and are shown in figure 2-13.

COUNTER/TIMER FUNCTION

The counter/timer function of the 7804A utilizes a three-channel, independently programmed 8253-5 counter/timer allowing multiple counting or timing operations to occur simultaneously. Each channel is supplied with several jumper selectable user options.

CLOCK

A 2-MHz clock signal to each channel is provided by the onboard CPU oscillator circuit. This clock signal is labeled CT0.

The user may disable the CT0 clock signal and provide an external clock signal for any or all of the counter/timer channels. First, remove the jumper corresponding to the appropriate channel; then add jumper W12 (figure 2-3) to allow access to the external clock signals. See figure 2-15 for proper jumper configuration.

NOTE

The maximum clock frequency the 8253-5 can accept is 2.5 MHz. Other versions of the 8253-5 that run at higher speeds may be available in the future.

CHANNEL	CLOCK	JUMPER INSTALLATION
2	Internal External	1-2* 3-4
1	Internal External	5-6* 7-8
0	Internal External	9-10* 11-12

* As Shipped

Figure 2-15. Internal/External Clock Jumper (7804A)

CONNECTOR J1

The connector on the card ejector side of the 7804A is for external connections to the counter/timer. It also provides one input line and one output line. A list of the pin numbers and their associated signals is shown in figure 2-16. The signal lines are described below.

Out 0, 1, 2: These output signals run from the three counter/timer channels to connector J1. Their output waveforms are described in section 3.

External Clock 0, 1, 2: As shipped, all three channels use the internal clock for down counting. Alternately, an external clock signal may be provided. There is a separate external clock input for each channel. The 8253-5 counter/timer accepts external clock signals up to 2.5 MHz.

Gate 0, 1, 2: Each channel has a gate for enabling the down counter. In some modes, the gate triggers the down counter, as with the hardware-triggered one-shot mode. In other modes, the gate must be held active continuously or the counter will stop. As shipped, the gates are held in the inactive state by a pull-up resistor. For the counter/timer to work in any of the modes, the gate must be either connected to an external signal or tied to ground. This prevents random activity by the counter/timer after power-up or reset.

Several shorting connectors are provided with the 7804A. They can be used to tie the gate to ground by connecting the gate to the ground line associated with it on the J1 connector. Refer to figure 2-16 for pin numbers of the ground lines.

External Status: This is a one-bit input port signal. It can be used for any purpose. In conjunction with the counter/timer, it is useful for reading back the output of a channel, etc.

External Control: This is a one-bit output port signal. It can also be used for any purpose. In conjunction with the counter/timer, it is useful for controlling the gate of a channel, etc. In addition, it can control the segment select input to the 7704 and 7705 memory cards, allowing the 7804A to access up to 256K bytes of memory.

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	2	EXT CONTROL*[1]
3	GROUND	4	GATE 2
5	GROUND	6	CLOCK 2
7	GROUND	8	OUT 2[1]
9	GROUND	10	GATE 1
11	GROUND	12	CLOCK 1
13	GROUND	14	OUT 1[1]
15	GROUND	16	GATE 0
17	GROUND	18	CLOCK 0
19	GROUND	20	OUT 0[1]
21	GROUND	22	EXT STATUS*
23	GROUND	24	SPARE
25	GROUND	26	SPARE

* Low-level active logic
[1] Open-collector driver

Figure 2-16. J1 Connector (7804A)

CIOCK OPTION

The clock for the Z80A and the 8253-5 counter/timer is generated by the 4 MHz hybrid clock circuit. Its output goes directly to the Z80A and also to a divide-by-two circuit before being applied to the 8253-5. The divide-by-two circuit is used because the 8253-5 cannot run at 4 MHz. If future versions of this chip become available that can run at this speed, jumper W14 can be removed from position 1-2 and placed in position 3-4 to bypass the divide-by-two circuit. Jumper W14 is shown in figure 2-3.

I/O DECODER

The I/O decoder selects the onboard I/O ports. It decodes the port address and generates a port select signal. There are two select signals for the two onboard ports, and one for the counter/timer. When the counter/timer select signal is generated, the counter/timer itself decodes address lines A0 and A1 to determine which of the four inherent ports is being selected. Also, a fourth line is generated that is part of the data bus control logic.

As shipped, the addresses of these six ports are F0-F5. They can be remapped to ports E8-ED by removing jumper W11, shown in figure 2-3. The functions and use of these ports are explained in section 3.

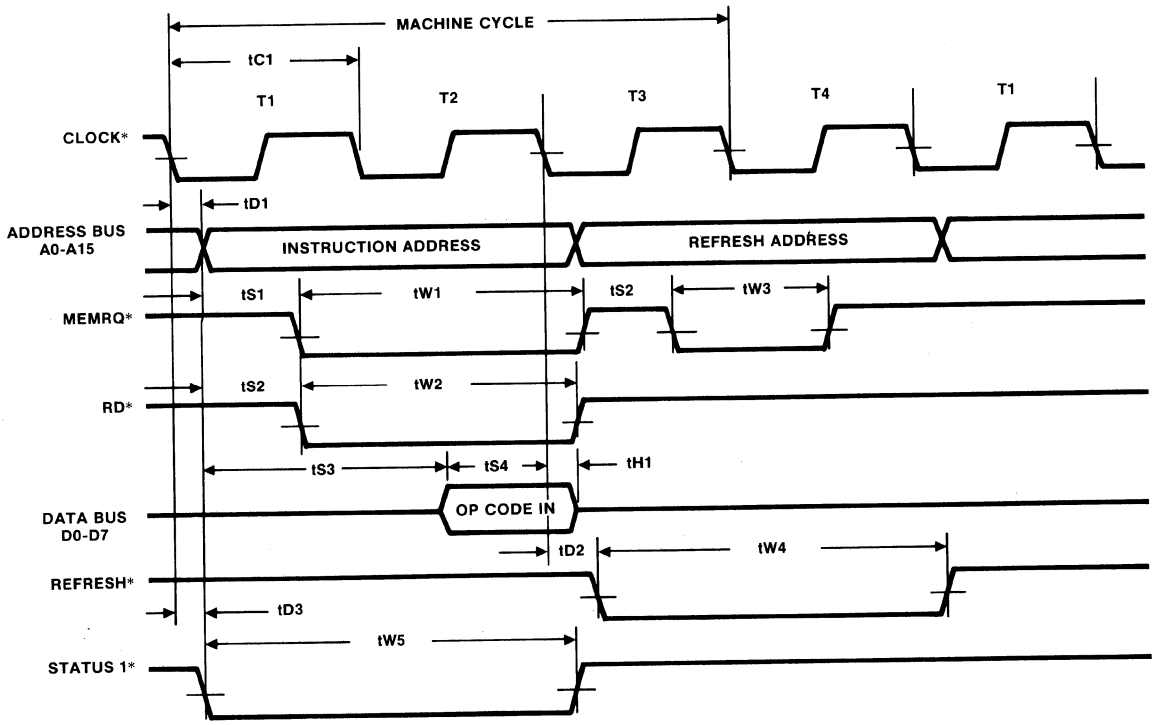
The I/O decoder is a PROM. If the onboard ports must be mapped to addresses other than those provided, replace the PROM with one containing your own program. If other addresses are used, the writing of the program and the programming of the PROM are the user's responsibility.

I/O EXPANSION

The IOEXP line, which is a part of the STD BUS, is tied to ground and cannot be controlled by the 7804A card. If you plan to use IOEXP, remove jumper W5. This leaves the line floating, allowing it to be controlled by some other card in the system. Jumper W5 is shown in figure 2-3.

TIMING SPECIFICATIONS

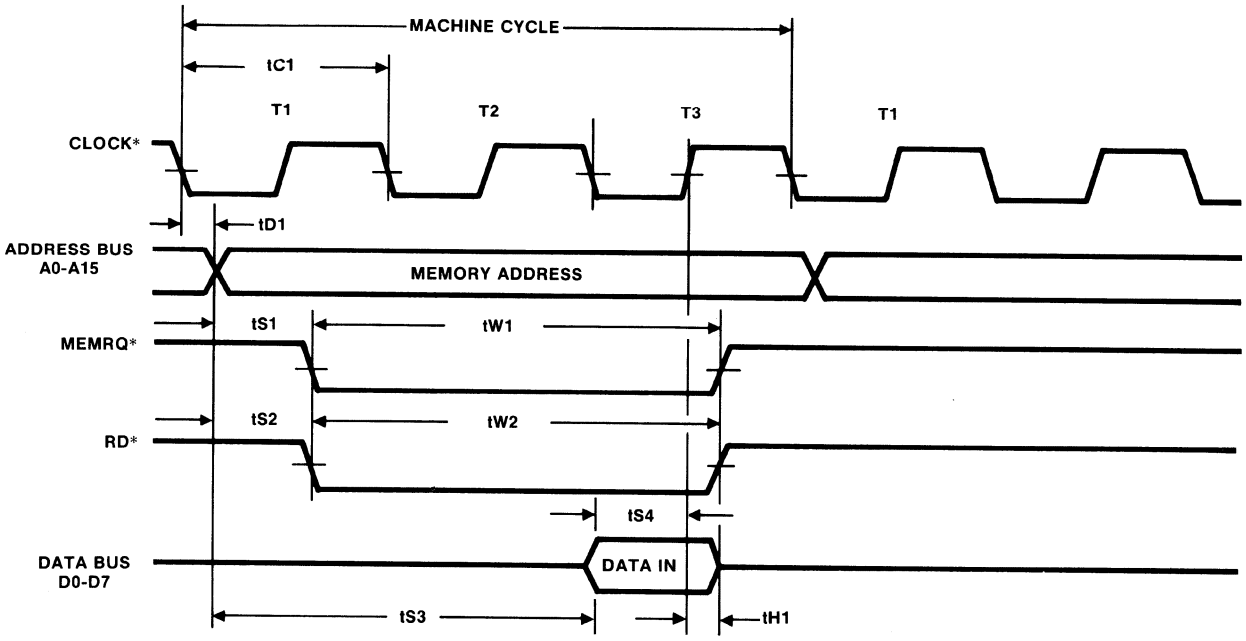
Figures 2-17 through 2-24 show the signal sequence and timing for various 7804A functions. They depict the signals as they appear at the card edge connector of the 7804A.



SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	Address delay from T1 clock	—	145	—	110
tD2	REFRESH* delay from start of T3	—	180	—	130
tD3	STATUS 1* delay from T1 clock ends	—	130	—	100
tH1	Data bus hold time after T2	0	—	0	—
tS1	Address setup before MEMRQ* active	125	—	65	—
tS2	Address setup before RD* active	195	—	125	—
tS3	Address setup before data valid	545	—	295	—
tS4	Data bus setup before T2 clock ends	70	—	70	—
tW1	MEMRQ* pulse width (OP code fetch)	500	—	290	—
tW2	RD* pulse width	470	—	280	—
tW3	MEMRQ* pulse width (refresh)	360	—	220	—
tW4	REFRESH* pulse width	620	—	370	—
tW5	STATUS 1* pulse width	670	—	400	—

All times given in nanoseconds
*Low-Level Active Logic

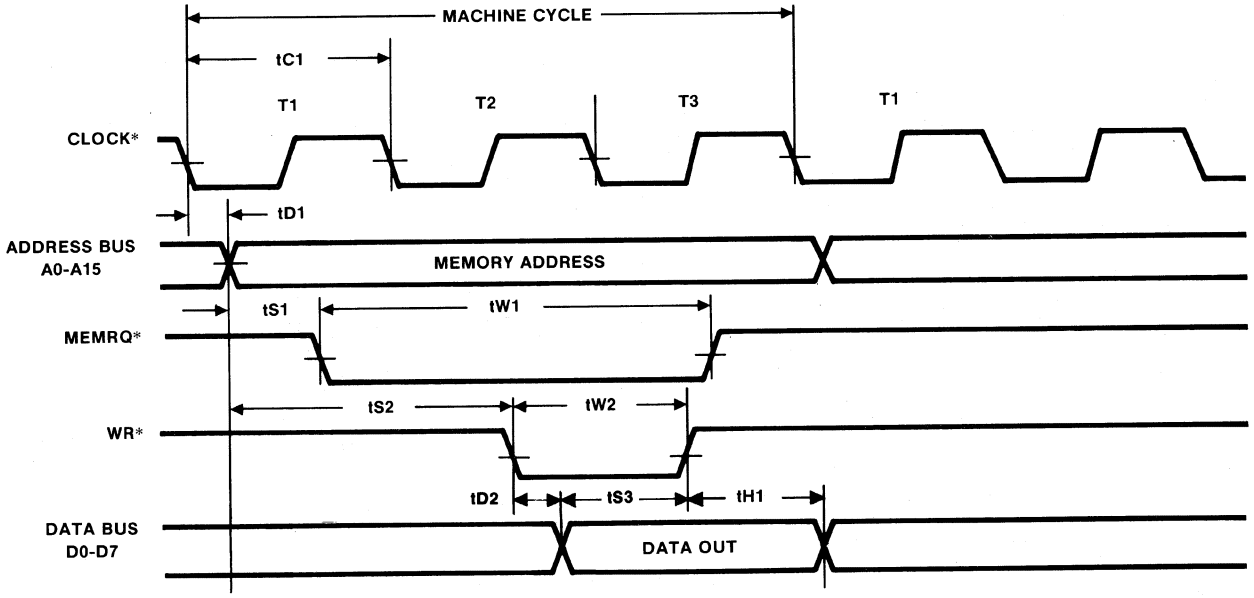
Figure 2-17. OP Code Fetch Timing and Refresh Timing (7804A)



SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	Address delay from T1 clock	—	145	—	110
tH1	Data hold time after clock high	0	—	0	—
tS1	Address setup before MEMRQ* active	135	—	75	—
tS2	Address setup before RD* active	185	—	110	—
tS3	Address setup before data valid	755	—	430	—
tS4	Data setup time before clock high	100	—	90	—
tW1	MEMRQ* pulse width	700	—	415	—
tW2	RD* pulse width	670	—	405	—

All times given in nanoseconds
*Low-Level Active Logic

Figure 2-18. Memory Read Timing Other Than OP Code Fetch (7804A)

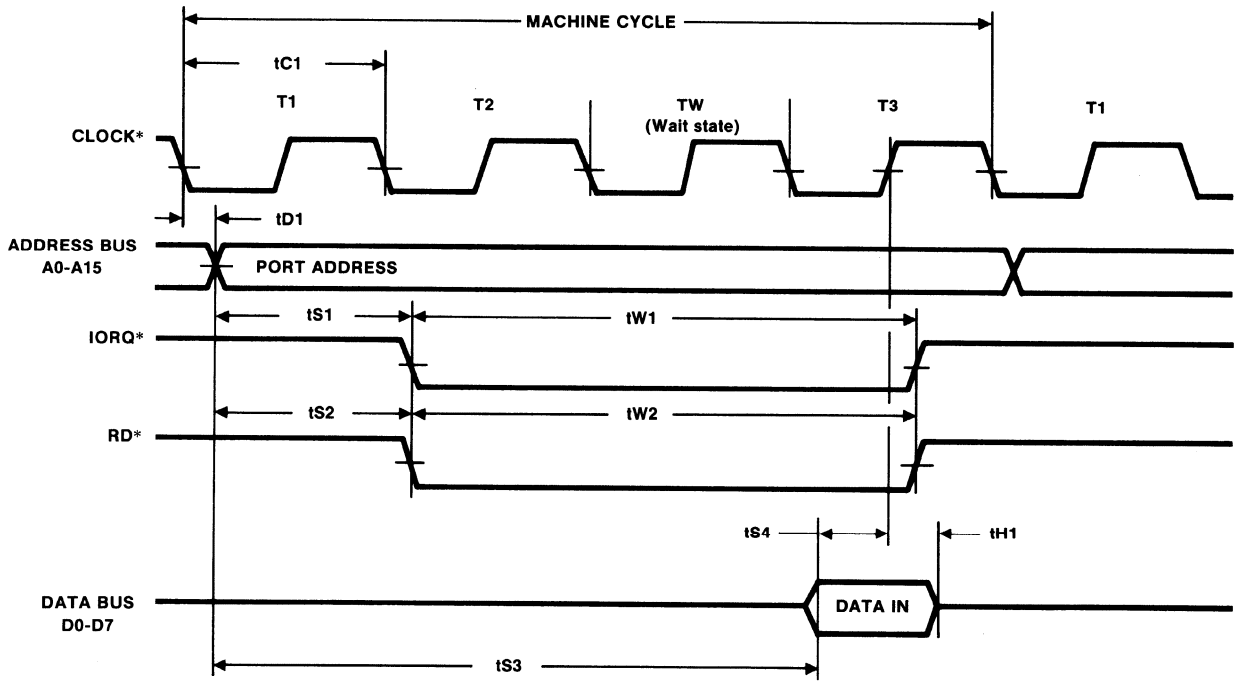


SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	Address delay from T1 clock	—	145	—	110
tD2	Data delay from WR* active	—	75	—	75
tH1	Data hold time after WR* ends	120	—	60	—
tS1	Address setup before MEMRQ* active	125	—	65	—
tS2	Address setup before WR* active	475	—	240	—
tS3	Data setup time before WR* ends	290	—	150	—
tW1	MEMRQ* pulse width	700	—	415	—
tW2	WR* pulse width	360	—	220	—

All times given in nanoseconds

*Low-Level Active Logic

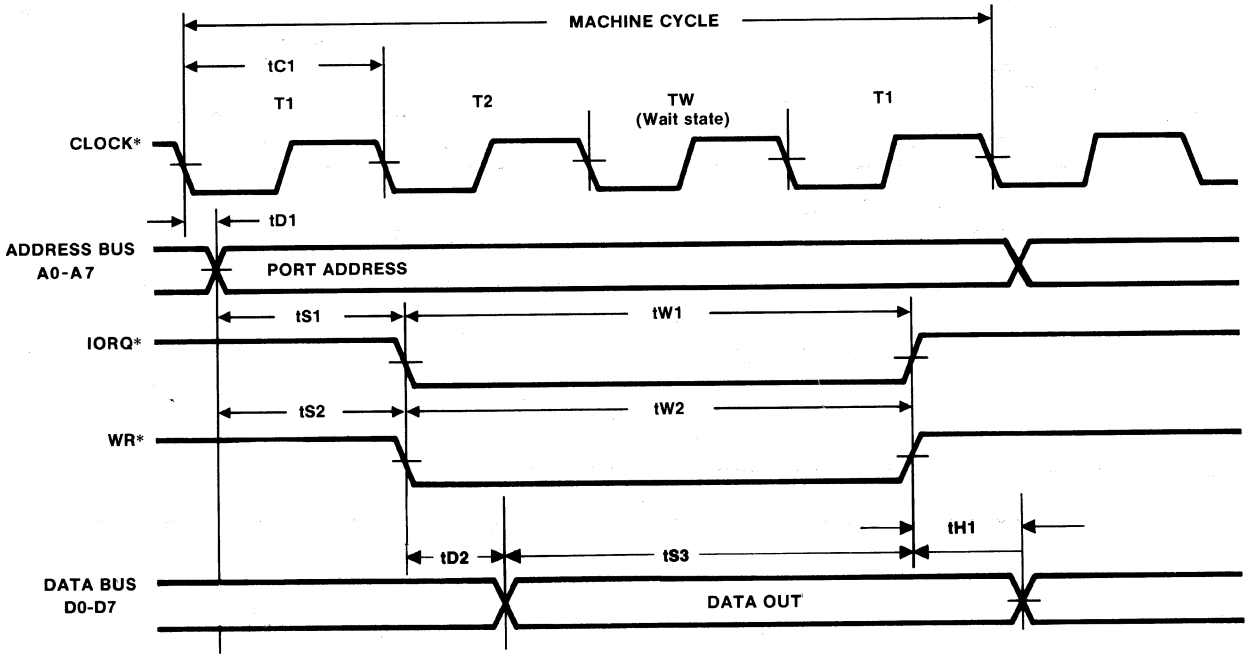
Figure 2-19. Write Timing (7804A)



SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	Address delay from T1 clock	—	145	—	110
tH1	Data hold time after clock high	0	—	0	—
tS1	Address setup before IORQ* active	320	—	180	—
tS2	Address setup before RD* active	355	—	190	—
tS3	Address setup before data valid	1175	—	600	—
tS4	Data setup time before clock high	80	—	70	—
tW1	IORQ* pulse width	890	—	540	—
tW2	RD* pulse width	890	—	540	—

All times given in nanoseconds
*Low-Level Active Logic

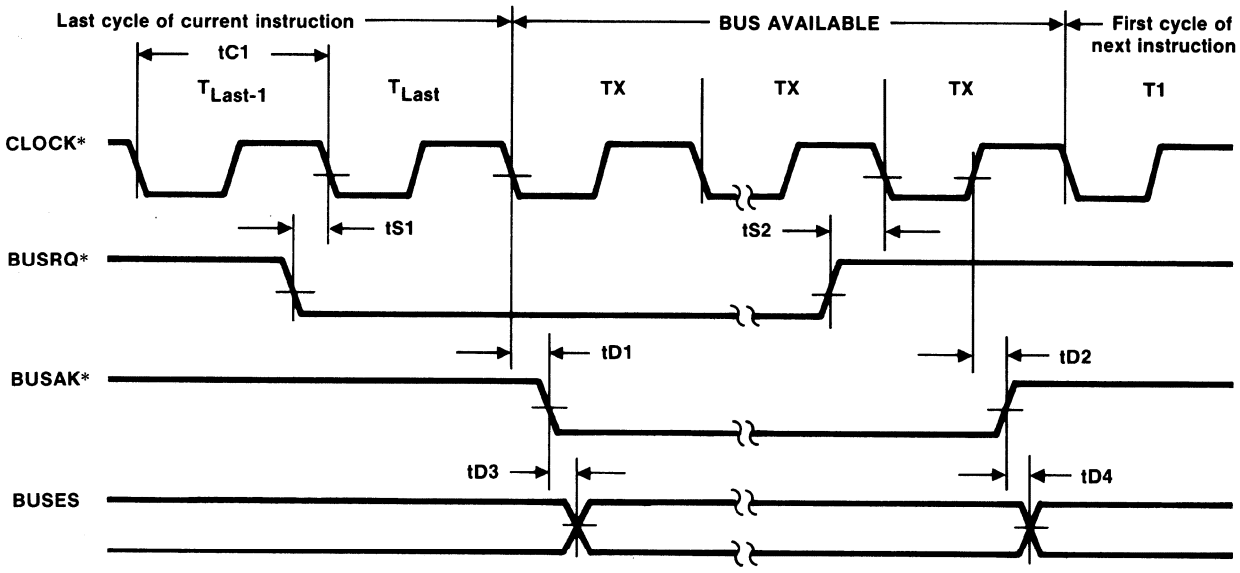
Figure 2-20. Input Timing (7804A)



SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	Address delay from T1 clock	—	145	—	110
tD2	Data delay from WR* active	—	75	—	75
tH1	Data hold time after WR* ends	0	—	0	—
tS1	Address setup before IORQ* active	320	—	180	—
tS2	Address setup before WR* active	335	—	205	—
tS3	Data setup before WR* ends	930	—	555	—
tW1	IORQ* pulse width	890	—	540	—
tW2	WR* pulse width	900	—	545	—

All times given in nanoseconds
*Low-Level Active Logic

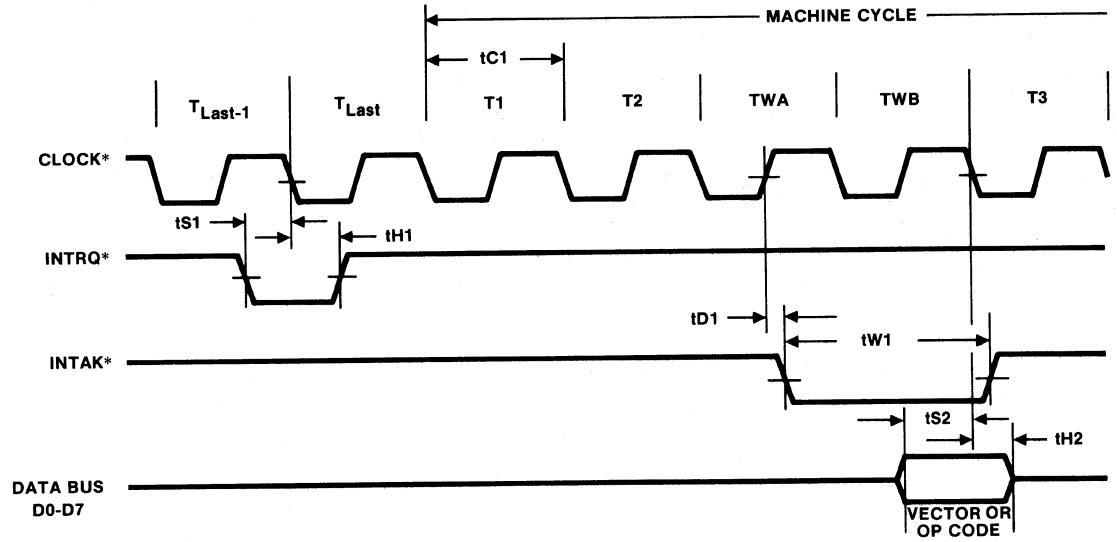
Figure 2-21. Output Timing (7804A)



SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	BUSAK* delay after start of first DMA cycle	—	140	—	120
tD2	BUSAK* delay after last DMA cycle	—	130	—	120
tD3	Buses delay after BUSAK* active	—	20	—	20
tD4	Buses delay after BUSAK* inactive	—	20	—	20
tS1	BUSRQ* setup prior to last time state	100	—	70	—
tS2	BUSRQ* release prior to sample	100	—	70	—

All times given in nanoseconds
*Low-Level Active Logic

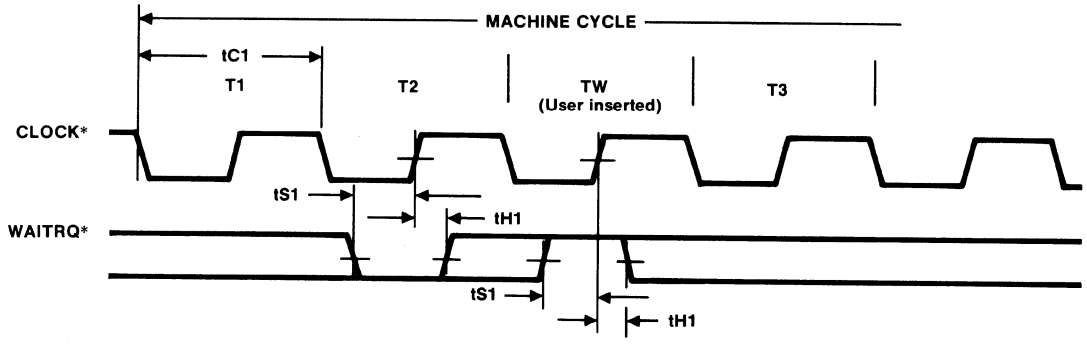
Figure 2-22. Bus Request Timing (7804A)



SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tD1	INTAK* delay after clock high	—	130	—	105
tH1	INTRQ* hold time after clock low	0	—	0	—
tH2	Data bus hold after clock low	0	—	0	—
tS1	INTRQ* set prior to last time state	100	—	100	—
tS2	Data bus setup before clock low	90	—	75	—
tW1	INTAK* pulse width	490	—	290	—

All times given in nanoseconds
*Low-Level Active Logic

Figure 2-23. Interrupt Request Timing (7804A)



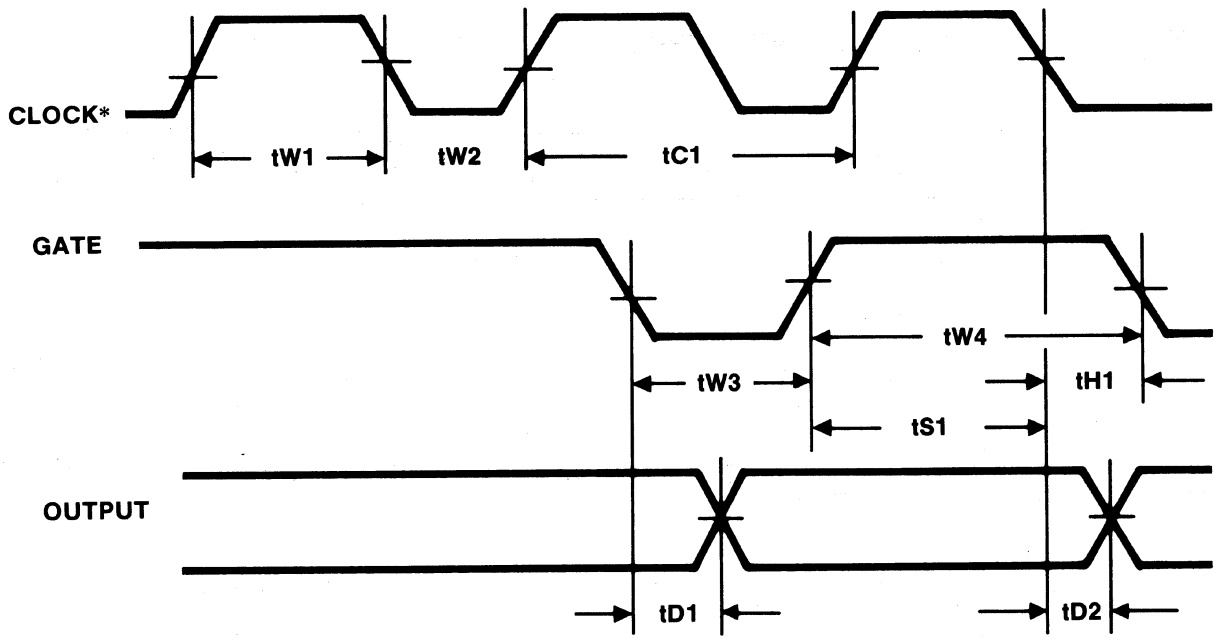
SYMBOL	PARAMETER	2.5 MHz		4.0 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock cycle time	400	—	250	—
tH1	WAITRQ* hold after clock high	0	—	0	—
tS1	WAITRQ* setup before clock high	90	—	90	—

All times given in nanoseconds
*Low-Level Active Logic

Figure 2-24. Wait State Timing (7804A)

COUNTER/TIMER TIMING SPECIFICATION

Figure 2-25 shows the relationship of waveforms at the user's interface connector J1. It depicts the minimum and maximum timing specifications that apply to the clock, gate, and output signals of any one of the three channels, over the specified VCC and operating temperature ranges.



SYMBOL	PARAMETER	4.0 MHz	
		MIN	MAX
tC1	Clock period asymmetrical waveform Clock period symmetrical waveform	400 500	— —
tD1	Output delay after gate	—	525
tD2	Output delay after clock	—	375
tH1	Gate hold time after clock	25	—
tS1	Gate setup time prior to clock	175	—
tW1	Clock high	250	—
tW2	Clock low	150	—
tW3	Gate low	125	—
tW4	Gate high	200	—

All times given in nanoseconds
*Low-Level Active Logic

Figure 2-25. User Interface Timing Specification (7804A)

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

MNEM	PARAMETER	UNITS	Recommended Operating Limits			Absolute Non-Operating Limits	
			MIN	TYP	MAX	MIN	MAX
Vcc	Supply Voltage	Volts	4.75	5.00	5.25	0	5.50
T_A	Free air operating temperature	°C	0	+25	+65	-40	+75
R_H	Humidity (noncondensing)	%RH	5	—	95	5	95

Figure 2-26. Electrical and Environmental Specifications (7804A)

MNEM	PARAMETER	UNIT	MIN	TYP	MAX
Icc	STD BUS supply current	mA	—	1000	1500[1]
—	STD BUS input load	See figure 2-28		See figure 2-28	
—	STD BUS output drive	See figure 2-28		See figure 2-28	

[1] With RAM/ROM sockets empty.

Figure 2-27. STD BUS Electrical Characteristics Over Recommended Operating Limits (7804A)

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	5	50	8	7	50	5	D3
D6	5	50	10	9	50	5	D2
D5	5	50	12	11	50	5	D1
D4	5	50	14	13	50	5	D0
A15	5	50	16	15	50	5	A7
A14	5	50	18	17	50	5	A6
A13	5	50	20	19	50	5	A5
A12	5	50	22	21	50	5	A4
A11	5	50	24	23	50	5	A3
A10	5	50	26	25	50	5	A2
A9	5	50	28	27	50	5	A1
A8	5	50	30	29	50	5	A0
RD*	5	50	32	31	50	5	WR*
MEMRQ*	5	50	34	33	50	5	IORQ*
MEMEX		OUT	36	35	OUT		IOEXP (GROUND)
MCSYNC*	5	50	38	37	50	5	REFRESH*
STATUS 0*			40	39	50	5	STATUS 1*
BUSRQ*	5	50	42	41	50	5	BUSAK*
INTRQ*	5	45	44	43	50	5	INTAK*
NMIRQ*	5		46	45		5	WAITRQ*
PBRESET*	1		48	47	50	5	SYSRESET*
CNTRL*			50	49	50	5	CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Low-level active logic

Figure 2-28. STD Edge Connector (7804A)

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	10[1]		EXT CONTROL*	1			GROUND
4		5	GATE 2	3			GROUND
6		5	CLOCK 2	5			GROUND
8	10[1]		OUT 2	7			GROUND
10		5	GATE 1	9			GROUND
12		5	CLOCK 1	11			GROUND
14	10[1]		OUT 1	13			GROUND
16		5	GATE 0	15			GROUND
18		5	CLOCK 0	17			GROUND
20	10[1]		OUT 0	19			GROUND
22		5	EXT STATUS*	21			GROUND
24			SPARE	23			GROUND
26			SPARE	25			GROUND

* Low-level active logic
[1] Open-collector driver

Figure 2-29. J1 Connector Counter/Timer (7804A)

MECHANICAL SPECIFICATIONS

The 7804A meets all general mechanical specifications of the STD BUS.

MATING CONNECTORS FOR THE INTERFACE CONNECTOR

Figure 2-30 lists the latching, 26-pin mating connectors for the header provided on the 7804A for the user's interface.

3M PART NO.	DESCRIPTION
3399-6000	Open end cover without strain relief
3399-6026	Open end cover with strain relief
3399-7000	Closed end cover without strain relief
3399-7026	Closed end cover with strain relief

Figure 2-30. J1 Mating Connectors (7804A)

JUMPER	DESCRIPTION	PAGE*
W1	Enable external MEMEX control	2-14
W2	Memory type socket 3	2-12
W3	Memory type socket 2	2-12
W4	Memory type socket 1	2-12
W5	Float IOEXP line	2-16
W6	Memory type socket 0	2-12
W7	Enable MEMEX for onboard memory (see also W1, W13)	2-13
W8	Memory map (see also W2,3,4,6,9, and 15)	2-3
W9	Disable unused sockets	2-13
W10	Disable 4 MHz clock	
W11	I/O port mapping	2-16
W12	3X internal/external clock for counter/timer	2-14
W13	Invert MEMEX	2-14
W14	Disable CTC clock prescaler	2-16
W15	Enable bootstrap	2-14
E1, E2	External system clock (W10)	

*Also refer to figure 2-3 for jumper locations.

Figure 2-31. Summary of Jumpers (7804A)

SECTION 3
Operation and Programming

INTRODUCTION

This section explains the operation and programmable functions of the 7804A card. The programmable functions are controlled by six onboard I/O ports. Figure 3-1 lists the port addresses and the functions. They are described separately in the order in which they are used most. The standard port addresses, F0-F5, are described in this section. To use the alternate port addresses, E8-ED, refer to the "I/O Decoder' subsection in section 2.

MEMEX

The MEMEX line, as part of the STD BUS, is for selecting between two banks of memory. Examples are given in figures 3-2 and 3-3. Figure 3-2 shows a system with 96K of memory. It has a 32K ROM, mapped at addresses 0000-7FFF, that does not respond to MEMEX and is permanently enabled. It also has a 64K RAM, broken up into two banks. Each bank has a 32K RAM. Both banks reside at addresses 8000-FFFF. One bank is enabled when MEMEX is high and one when it is low.

Figure 3-3 shows a system with 128K of memory in two 64K banks. The processor can choose which bank to work with by setting the MEMEX line high or low. These are just two examples of the many different applications of MEMEX.

MEMEX is usually controlled by either an I/O port or a memory segment controller. The port or controller can be on the processor card or on some other card in the system. In the case of the 7804A card, output port F5 on the card controls MEMEX. Port F5 is a one-bit data latch that latches out data bit 0.

PORT ADDRESS AS SHIPPED WITH JUMPER W11 INSTALLED	PORT ADDRESS WITH JUMPER W11 REMOVED	INPUT FUNCTION	OUTPUT FUNCTION
F0	E8	Read counter/timer Channel 0	Load counter/timer Channel 0
F1	E9	Read counter/timer Channel 1	Load counter/timer Channel 1
F2	EA	Read counter/timer Channel 2	Load counter/timer Channel 2
F3	EB	Not Used	Counter/timer Mode control
F4	EC	Counter/timer Interrupt status External status	Counter/timer Interrupt control External control Bootstrap control
F5	ED	Not Used	MEMEX Control

Figure 3-1. Onboard Ports and their Functions (7804A)

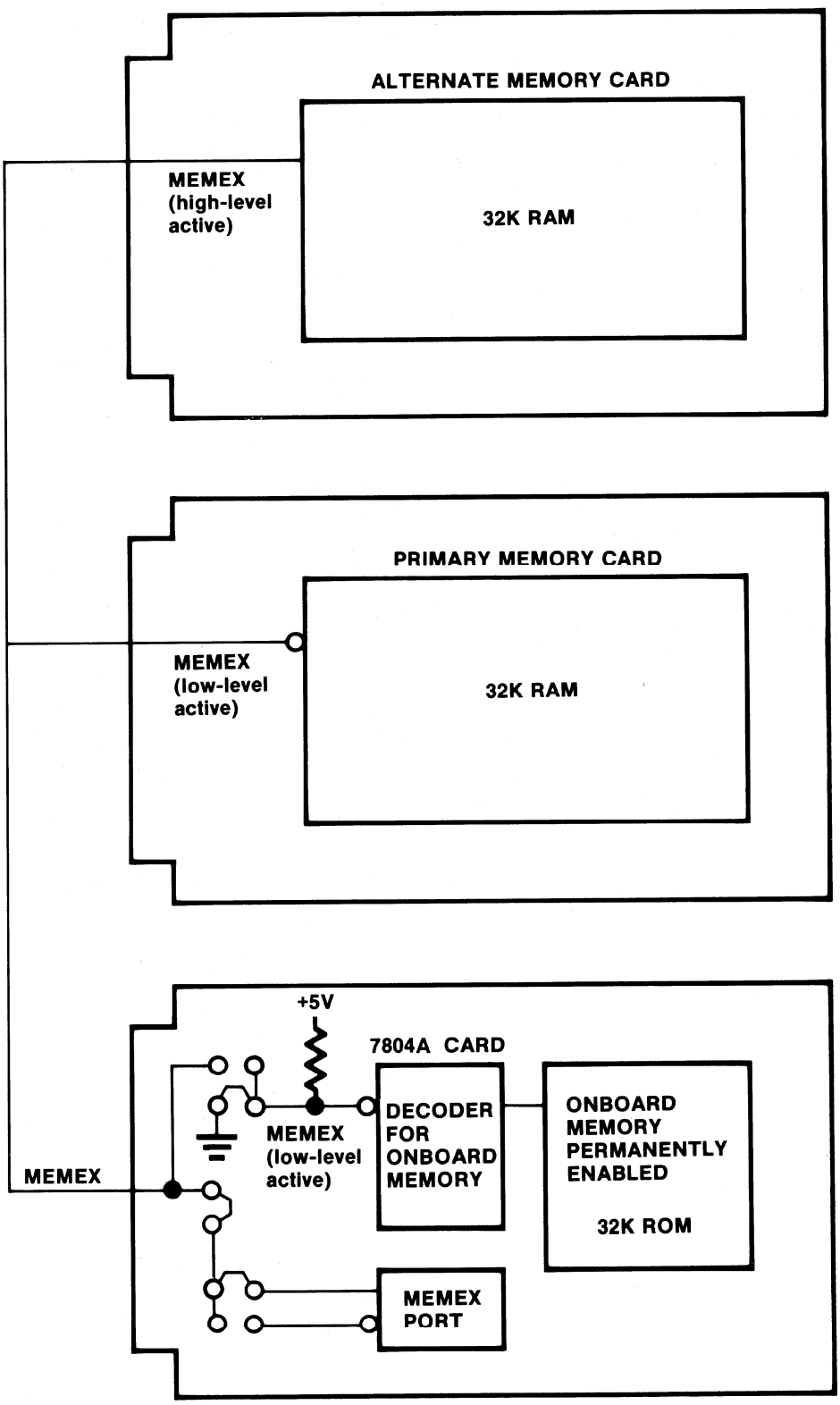


Figure 3-2. Example of MEMEX for Selecting Between Two Banks of Memory in a 96K Memory System (7804A)

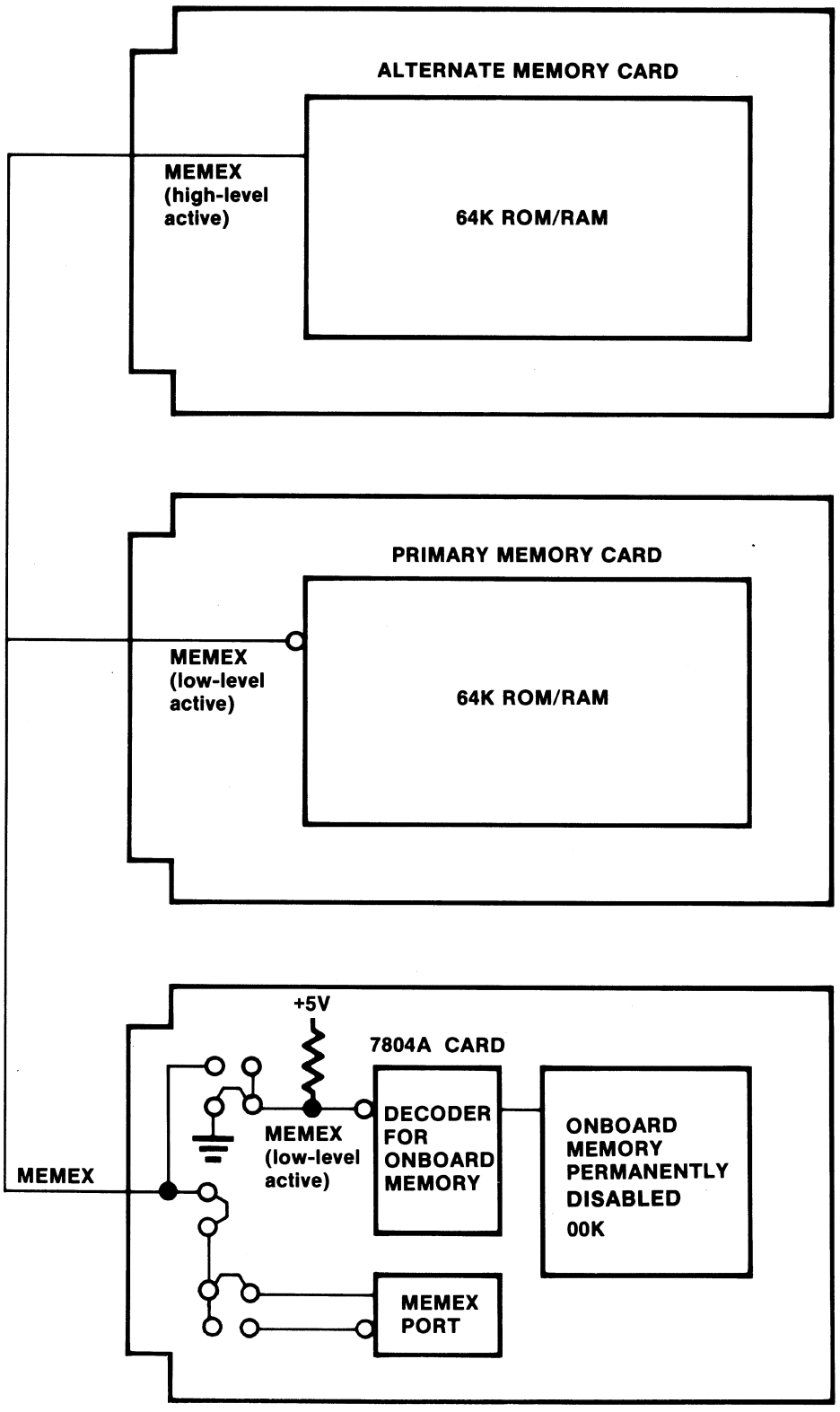


Figure 3-3. Example of MEMEX for Selecting Between Two Banks of Memory in a 128K Memory System (7804A)

BOOTSTRAP

The bootstrap function is an option allowing the processor to start at address F000 rather than at address 0000 after power-up or PBRESET*. Its implementation is explained in section 2.

Once this option is implemented, the most significant four address lines are set high after power-up or reset and they stay high until released. This means until they are released the processor can only access addresses F000-FFFF. The address lines are released by an onboard output port. The least significant data bit of port F4 is used for this purpose. To release the upper four address bits, a logic 1 is written out.

A program listing of how your software should control the bootstrap function is exemplified in figure 3-4.

The bootstrap function is suitable in systems using mass storage devices such as disks. The program in the bootstrap PROM loads an operating program from the disk into RAM. The operating program can then control the disk and other functions of the system. All of the lower addresses, 0000-EFFF, can be loaded with RAM, which can then run programs loaded from the disk.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE BOOT STRAP — DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
F0	00	C3		JP	UN	JUMP UNCONDITIONAL TO ADDRESS
	1	03		—		F003
	2	F0		—		
	3	3E		LDAI		RELEASE MOST SIGNIFICANT 4 ADDRESS LINES
	4	01		—		BY WRITING BIT 0, PORT F4, HIGH (LOGIC 1)
	5	D3		OPA		
	6	F4				
	7					USER'S PROGRAM STARTS HERE
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-4. Software Example of Bootstrap Option (7804A)

DIRECT MEMORY ACCESS

The DMA function permits another processor in the system, or some peripheral card, to request the processor to release the address, data, and control buses, and allow the external device direct access to memory. On the 7804A the DMA allows access to both external memory and onboard memory.

To give the external device DMA, the external device must generate a BUSRQ* signal, which is a part of the STD BUS. Figure 2-22 shows the required signal timing. Figure 3-5 shows the sequence of events for all affected signals. It is not intended to depict accurate timing or logic. As revealed in figure 3-5, the Z80A samples the BUSRQ* signal at the start of the last time state in any machine cycle. It responds by generating a BUSAK* signal and releasing the bus at the start of the next time state. The BUSAK* signal, also part of the STD BUS, can be used by the external device to determine when the bus is available.

Bus release occurs as follows. The address bus is enabled in so that onboard memory can be accessed by the external device. The data bus comes under the control of the external device. It is enabled in for read or write operations to external memory, or for write operations to onboard memory. It is enabled out for read operations from onboard memory.

The MCSYNC*, INTAK*, and STATUS 1* signals go into a high impedance state. Normally the MEMEX line is affected in the same way, except when it is being controlled by some other card in the system or if onboard memory is set up to respond to MEMEX. In the latter case, a pull-up resistor connected to jumper W7 holds the line high. In any case, ensure that the MEMEX line is in the proper state for any MEMEX-dependent memory you want to access.

The RD*, WR*, MEMRQ*, and IORQ* lines are enabled in so that the external device can control onboard memory. This occurs at approximately the same time BUSAK* goes active. The exact timing is shown in figure 2-22. Do not allow these lines to go into a random condition since they will be floating on the backplane. This condition is prevented by providing pull-up resistors for these lines on the external device card, holding these lines in the inactive state until the external device begins to use them.

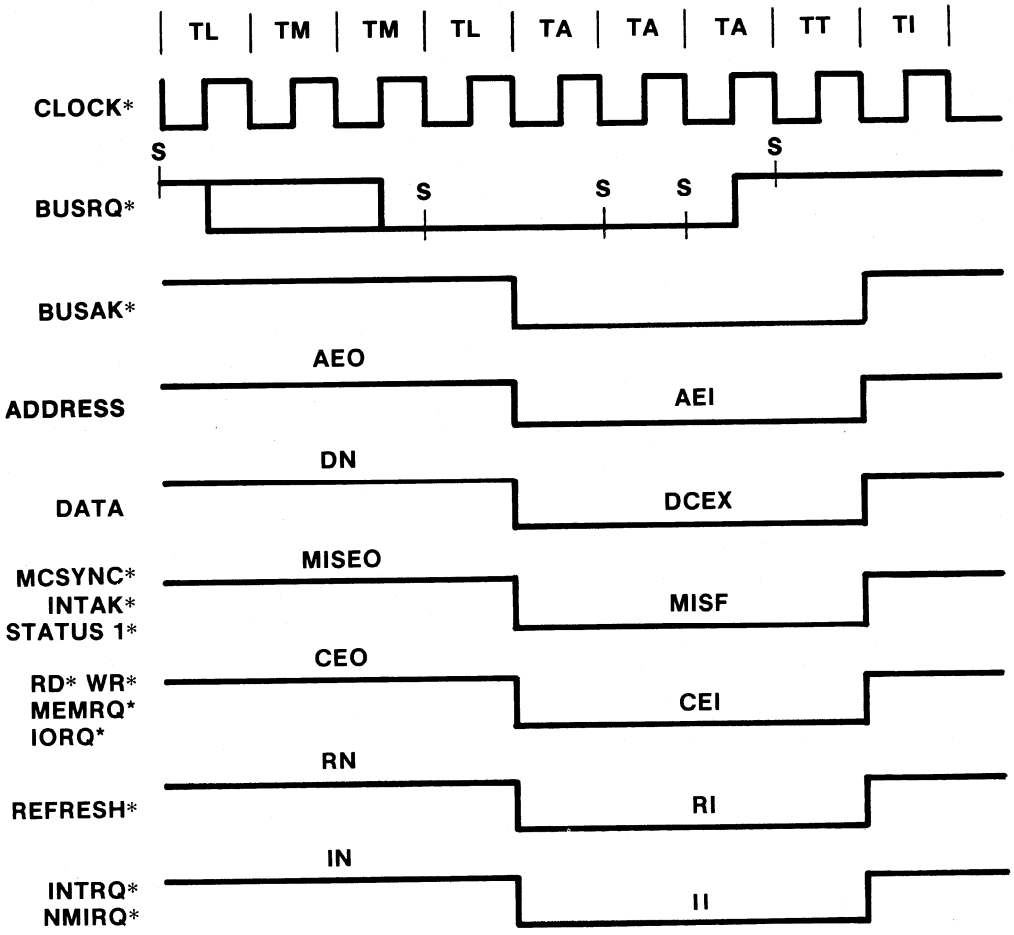
Clock* and SYSRESET* are not affected.

REFRESH* goes into its inactive state, which means that dynamic RAM cannot be refreshed during this time. The Z80A's refresh counter stops so that REFRESH* can pick up where it left off after the operation.

The processor stays in its suspended condition until BUSRQ* goes inactive. BUSRQ* is sampled at the beginning of each time state. BUSAK* goes inactive and the buses return to normal during the first time state that BUSRQ* is found inactive. With the next time state, the processor continues where it left off.

During DMA operations, no interrupts can be acknowledged and they are serviced only when the processor returns to its normal operation.

TL	=	Last time state of any machine cycle
TM	=	Misc. time states of any machine cycle, may be 2 to 5 time states
TA	=	Time states during which bus is available
TT	=	Time state during which transition is made back to normal operation
TI	=	First time state of next machine cycle



S	=	BUSRQ* sampled
AEO	=	Address bus enabled out
AEI	=	Address bus enabled in
DN	=	Data bus normal operation
DCEX	=	Data bus under control of external device
MISEO	=	MCSYNC*, INTAK*, and STATUS 1* are enabled out
MISF	=	MCSYNC*, INTAK* and STATUS 1* floating
CEO	=	Control lines enabled out
CEI	=	Control lines enabled in
RN	=	REFRESH* normal operation
RI	=	REFRESH* inactive
IN	=	Interrupts normal operation
II	=	Interrupts ignored

Figure 3-5. Bus Request Sequence — DMA Function (7804A)

COUNTER/TIMER

The counter/timer is a multi-channel, programmable function. Its uses include:

- Event counting
- Square-wave and marker-pulse waveform generator
- One-shot simulation with hardware and software triggering and retriggering
- Timed interrupts
- Input of external interrupts

Counter/Timer Channels

The main elements of the counter/timer function are the three independent channels. These channels are similar in logical organization. See figure 3-6 for a single-channel block diagram. Each channel consists of:

- A 16-bit counter (down counter)
- 16-bit channel read and load registers
- Mode control registers (6 bit)
- Onboard 2 MHz clock control or external clock control option
- TTL-buffered gate control available at user's connector (J1)
- TTL-buffered output available at user's connector (J1)
- Interrupt control circuit

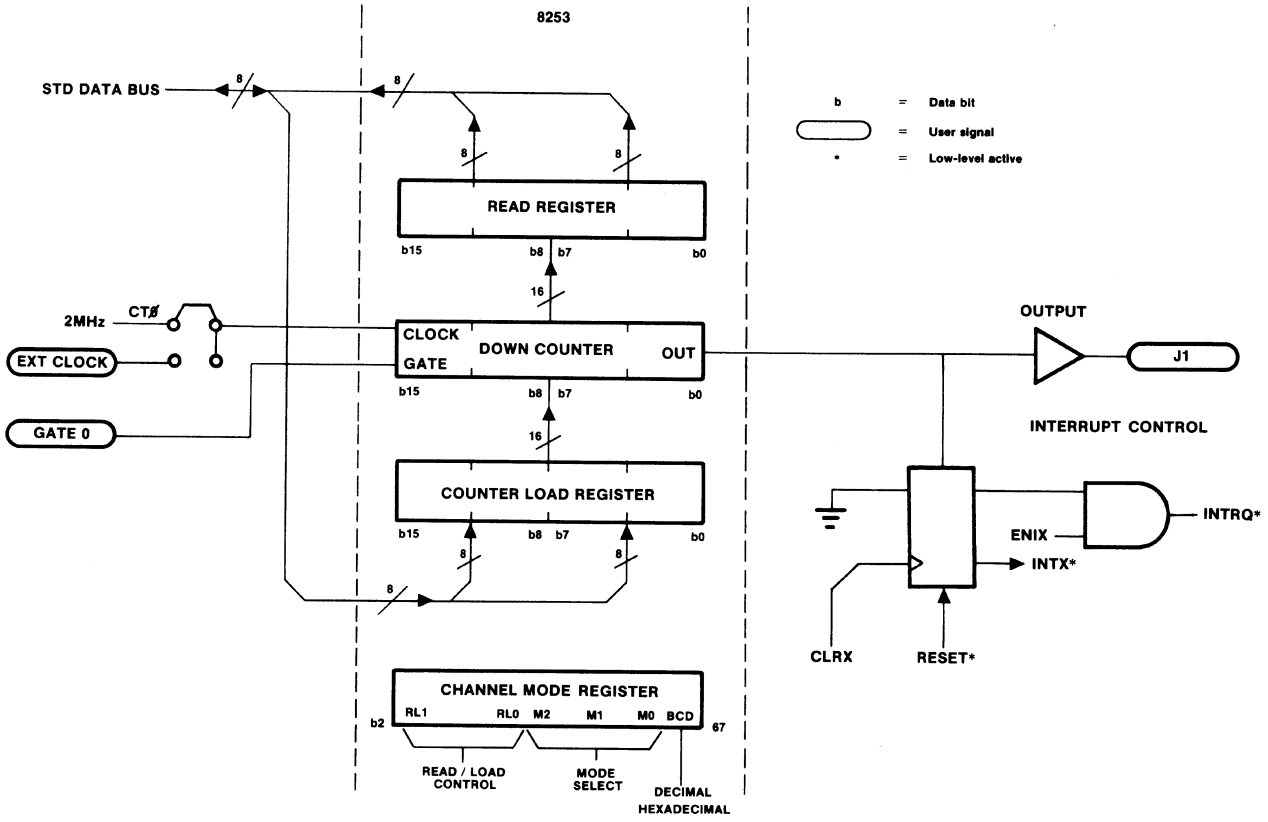


Figure 3-6. Block Diagram of a Single Channel of the 8253-5 Counter/Timer (7804A)

Down Counter, Load Register, and Read Register

The central element in each channel is the **16-bit down counter.** Remaining logic elements control and monitor the down counter and set its mode of operation.

The down counter can be preset to any value in the range of 0000-FFFF (hexadecimal) or 0000-9999 (decimal). Once all of the preset input conditions are met, the down counter decrements with each transition at its CLOCK input until **terminal count** is reached.

Terminal count is defined as the lowest number obtainable when down counting. Depending on mode, this may be 0000, 0001, or 0002 (decimal or hexadecimal). When terminal count is reached, the OUTPUT circuit responds according to its mode selection.

The down counter is preset to any desired value through the 16-bit latching **load register**. Note that the program can only write to the load register, not to the down counter itself.

The preload value written to the load register does not enter the down counter immediately. Instead, it is clocked in by the first active transition of the counter/-timer clock. In some modes, this does not happen until the gate goes active. This is explained in the description of the counter/timer modes (figures 3-12 through 3-17).

The register used to read the counter operates in one of two modes. One is the transparent mode in which the register's output tracks the down counter's output exactly and no latching action occurs. The other mode is the latched mode in which it synchronously latches the counter's current output upon program command. In the latched mode, internal gating synchronizes the read register and the down counter so the read register does not latch until the down counter is stable. Thus a misread of the down counter from the ripple effect of carry propagation across the 16 bits cannot occur within the clock rate specifications.

Mode Control Registers

Each 16-bit counter/timer channel has an associated 6-bit mode control register. Use the register to program different modes of operation for each channel, allowing the channels to operate independently with no interaction.

The mode control registers select the following parameters:

- One of six operating modes:
  0. Single count, single delay, software-triggered one-shot
  1. Hardware-triggered one-shot or count, retriggerable
  2. Rate generator or divide-by-N counter with autoreload
  3. Square wave generator
  4. Software-triggered strobe
  5. Hardware-triggered strobe, retriggerable
- One of three read/load formats for counter data
- Transparent or latched data readback
- Binary or BCD (hexadecimal or decimal) down counting

The data bus available to the 8253-5 is 8 bits wide, but each counter/timer channel is 16 bits wide. Consequently, a protocol must be established to handle writing to, and reading from, the counters. The mode register performs this function. It also controls the transparent or latched characteristics of the read register and establishes the basic operating mode for the channel (single count, one-shot, marker generator, etc.).

> **NOTE**
>
> Writing to the mode control register immediately cancels the channel's current operation. This occurs even if identical bit states are rewritten to bits 0-3 of the mode control register. After a write to the mode control register, channel operation cannot resume until a preset value is written to the channel's load register.
>
> There is a single exception to this rule. The channel's read register can be changed from transparent mode to latched mode without cancelling the channel's operation, provided no other mode control register bits change.

The format and function of the mode control register's bits are shown in figure 3-7. They are defined in detail in the discussion that follows.

FUNCTION	ADDRESS		TRANSFER PROTOCOL		MODE CONTROL			HEXADECIMAL/ DECIMAL
Mnemonic	SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Data bit	b7	b6	b5	b4	b3	b2	b1	b0

Figure 3-7. Mode Control Format - Counter/Timer Channels (7804A)

SC1	SC0	CHANNEL
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Illegal

Figure 3-8. Bit Combination for Channel Selection (7804A)

RL1	RL0	READ/LOAD PROTOCOL
0	0	Latched read mode
0	1	Lower byte only
1	0	Upper byte only
1	1	Lower byte, then upper byte

Figure 3-9. Bit Combination for Read/Load Protocol Selection (7804A)

M2	M1	M0	MODE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	2 (Duplicate)
1	1	1	3 (Duplicate)

Figure 3-10. Bit Combination for Operating Modes (7804A)

BCD	HEXADECIMAL/DECIMAL
0	Hexadecimal
1	Decimal

Figure 3-11. Bit Selection for Decimal/ Hexadecimal Operations (7804A)

Select Channel: Bits SC0 and SC1

These two bits select the mode control register for one of the three channels. Figure 3-8 shows the required bit combination for each channel.

Read/Load Format: Bits RL0 and RL1

These two bits select one of four modes for communicating with the 16-bit channels from an 8-bit data bus. The combination for each mode is shown in figure 3-9.

Mode 00 is never used when initializing a channel. It is used only after the channel is initialized to read the current count in the counter. When initializing a channel, choose one of the other three modes. This establishes a protocol for reading and writing to the channel that remains the same even if the latched read mode is selected later.

In mode 11, it is important to read or write two bytes to the channel whenever a transfer is performed. The least significant byte is transferred first, followed by the most significant byte. When writing a number to the channel to preset the counter, the counter will not start until it has been given both bytes. When reading a count, both bytes must be read before a new count can be read; however, this sequence can be cancelled at any time by selecting a new mode.

Mode Select: Bits M0, M1, M2

These three bits select one of six possible operation modes. See figure 3-10 for the required bit combination for each mode.

Binary or BCD (Hexadecimal or Decimal) Counting: Bit BCD

This bit allows the down counter to operate in binary or decimal counts. A"0" bit sets the down counter in binary or hexadecimal operation. A "1" bit sets the down counter in decimal operation. See figure 3-11.

Read Mode

The processor reads the content of any counter/timer channel in one of two ways: transparent mode or latched mode.

When in the transparent mode, the real-time value of the counter is visible to the processor. The transparent mode is selected when the RL bits are 01, 10, or 11. This is the initial mode for reading since the channel can't be preloaded to an initial count value without selecting one of these combinations. Once set to 01, 10, or 11 the channel remembers the selection. The processor can then change to RL = 00 and select the latched mode.

If the processor is halted by a logic analyzer while in the act of reading one of the counter/timer channels in the transparent mode, each CLOCK transition causes a new count to appear on the STD data bus. By this method the counting operation can be monitored directly.

In the latched mode, writing RL = 00 to the mode control register creates a dynamic read strobe that synchronously latches the channel's count into the associated read register. The next time the processor reads the count it actually reads the output of the latched read register. This avoids the possibility of read errors introduced by asynchronous carry propagation across the 16-bit counter during the act of reading. The read register remains latched while the processor reads one byte or two bytes (according to the previous state of the RL bits). After being read, the read register returns to the transparent mode. This sequence, writing RL = 00 and reading the count, must be repeated each time a latched count is read.

The transparent mode is useful only when counting external events that happen at a relatively slow rate. You should have enough time to take two readings between counts. This prevents misreadings. A misreading can occur if you read the count while it is changing. To avoid this, read the count twice and compare the two readings. If they are the same, you can assume that it is a valid reading.

Sequence of Operations in Each Mode

Figures 3-12 through 3-17 describe the waveforms and the sequence of operations in each of the six operating modes. The signals at the user's interface connector J1 will match the waveforms shown on the following pages.

In all modes, the channel's output assumes a defined state immediately after the rising edge of the WR* signal when the mode control register is loaded with the new mode. An output transition can occur at this time, depending on the output state remaining from the previous mode. Do not inadvertently generate an interrupt at this time. Prevent it by setting the channel control port's interrupt enable bit ENI = 0 (until the new mode is selected and the output state is known).

In describing the modes, we use these conventions:

- GATE, CLOCK, and OUTPUT are capitalized when they refer to one of the channel's input/output signals appearing at the user's interface connector J1.
- A signal available to the user is denoted by ⊂⊃.
- Low-level active logic is denoted by an asterisk (*).

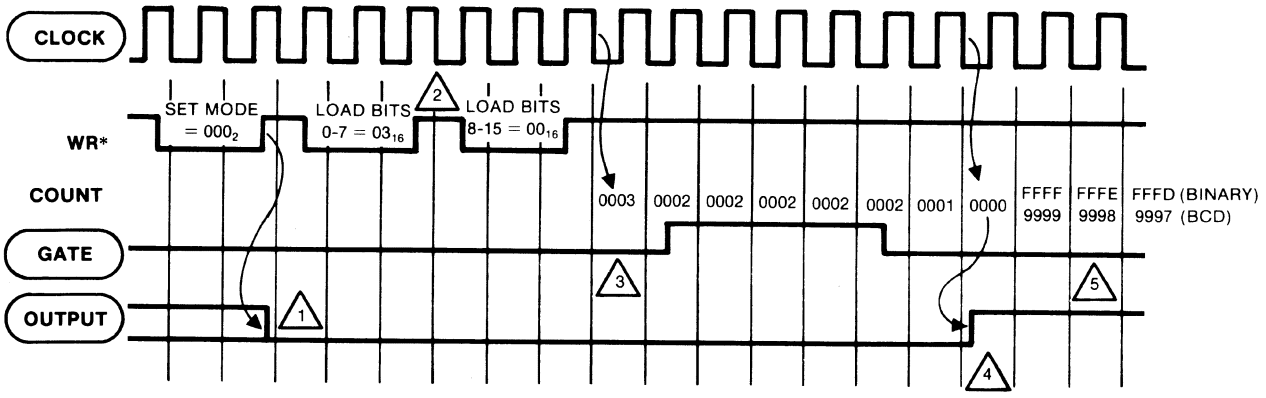


Figure 3-12. Counter/Timer Mode 0—Single Count, Single Delay, Software-Triggered One-Shot (7804A)

1 OUTPUT goes active (low) with the rising edge of WR* when Mode 0 is selected; counting stops regardless of CLOCK or GATE activity, and the count remaining from the previous mode is frozen in the counter. As a software-triggered one-shot, OUTPUT goes active when Mode 0 is first selected and stays active until terminal count. Thereafter, as long as Mode 0 remains selected, OUTPUT goes active (one-shot is retriggered by software) when the first byte of the preload value is written in the load register.

2 Counting cannot resume until one or two bytes of preload data (initial value) are written to the load register. The state of the mode control register's RL bits determines whether one byte or two bytes are needed. CLOCK transitions occuring between write cycles are irrelevant until the channel is preloaded.

3 After the preload operation, the first CLOCK falling edge, with GATE active, transfers the preload value from the load register to the counter. Subsequent CLOCK falling edges decrement the count. GATE can be used to modulate the count if desired. Counting can only occur while GATE is active. For an initial count of 0001, GATE has no effect on OUTPUT. If Gate is used to stop counting, GATE must be assured of going inactive at least two full clock cycles before terminal count to prevent OUTPUT from going inactive. GATE can stop the counter content at a value of 0001, but it cannot prevent OUTPUT from going inactive with the next CLOCK edge.

4 Terminal count for Mode 0 is 0000 (decimal or hexadecimal). Immediately after the clock terminal count, OUTPUT goes inactive (high) and remains inactive until a new mode is selected.

5 After terminal count, the channel continues to decrement past 0000 according to the state of the BCD mode bit. The preload value is never reloaded to the counter. The only way to exit from Mode 0 is to write a new mode selection into the channel's mode control register.

NOTE

The waveforms above show an example in which the load register is preset to the initial value 0003 (decimal or hexadecimal). WR* is an STD BUS signal (pin 31) which is active with IORQ* (pin 33) and IOEXP (pin 35) during an output-port write operation.

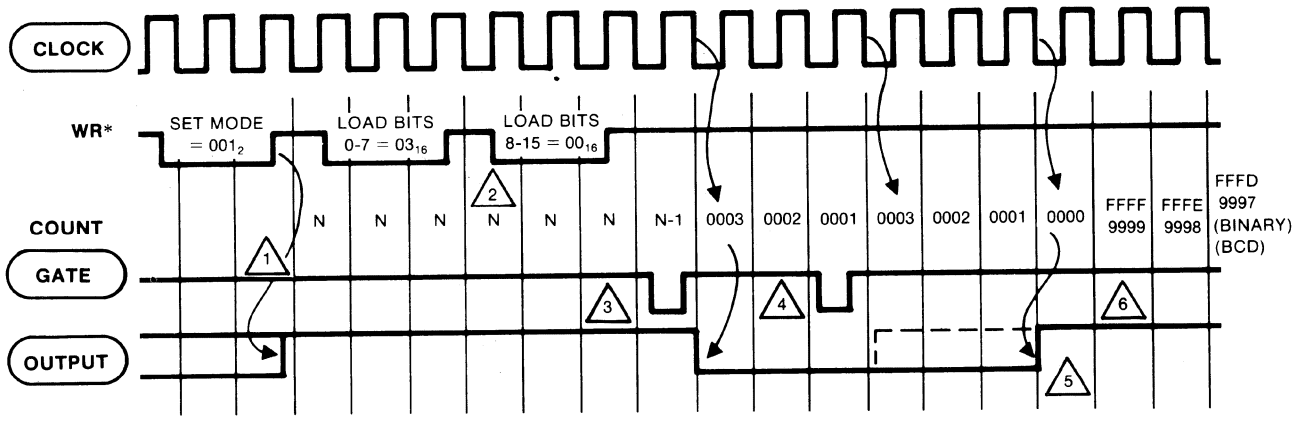


Figure 3-13. Counter/Timer Mode 1—Hardware Triggered, One-Shot or Count, Retriggerable (7804A)

1 OUTPUT goes inactive (high) with the rising edge of WR* when Mode 1 is selected; counting stops regardless of CLOCK or GATE activity, and the count remaining from the previous mode (N) is frozen in the counter.

CAUTION

Disable GATE by setting GTE = 0 in the program before selecting Mode 1 and do not reenable GATE until the preload value has been loaded. This prevents inadvertent OUTPUT activity.

2 Counting cannot resume until one or two bytes of preload data (initial value) are written to the load register. The state of the mode control register's RL bits determines whether one byte or two bytes are needed. CLOCK transitions occurring between write cycles are irrelevant until the channel is preloaded.

Once the channel's initial value is set, CLOCK transitions decrement the counter regardless of the state of the GATE. However, counting proceeds from the value N (to N-1, N-2 ...) left in the counter from the previous mode.

3 GATE's falling edge triggers the Mode 1 one-shot action. The next CLOCK falling edge, after the GATE edge, transfers the preload value from the load register into the counter and sets OUTPUT active (low). After triggering the count, GATE may remain high or low without affecting the one-shot action.

4 If another GATE edge trigger occurs before terminal count, the one-shot is retriggered; the preload value is again transferred from the load register to the counter on the next CLOCK falling edge; counting proceeds from the preload value; OUTPUT remains active (low) without glitching.

5 Terminal count for Mode 1 is 0000 (decimal or hexadecimal). Immediately after the CLOCK edge causing terminal count, OUTPUT goes inactive (high) and remains inactive until a new mode is selected.

6 After terminal count, the channel continues to decrement past 0000 according to the state of the BCD mode bit. Decrementing continues freely with each CLOCK edge until the next GATE trigger.

NOTE

The waveforms above show an example in which the load register is preset to the initial value 0003 (decimal or hexadecimal). WR* is an STD BUS signal (pin 31) which is active with IORQ* (pin 33) and IOEXP (pin 35) during an output-port write operation.

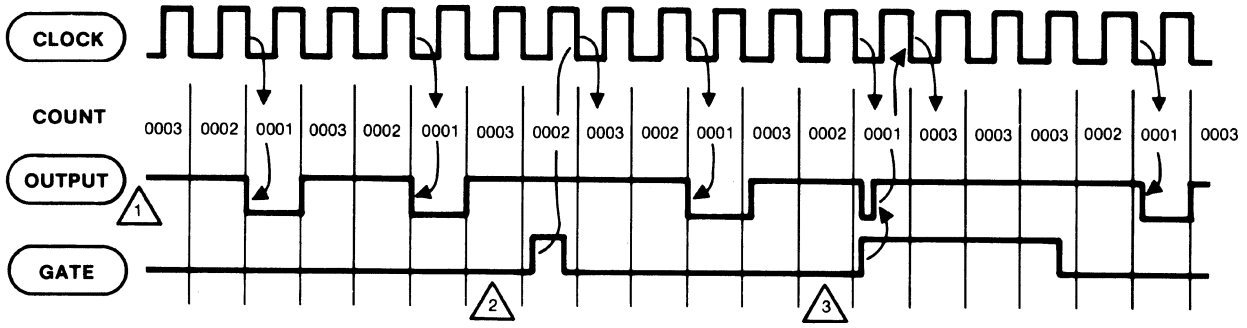


Figure 3-14. Counter/Timer Mode 2—Rate Generator or Divide-by-N Counter with Auto-Reload (7804A)

1 OUTPUT goes inactive (high) with the rising edge of WR* when Mode 2 is selected; counting stops regardless of CLOCK or GATE activity, and the count remaining from the previous mode is frozen in the counter. In the waveforms above, 0003 (decimal or hexadecimal) has been preloaded after the selection of Mode 2 as an example.

If GATE is high after the preload operation, the first CLOCK falling edge transfers the preload value from the load register to the counter, and subsequent CLOCK falling edges decrement the count toward terminal count.

Terminal count for Mode 2 is 0001 (decimal or hexadecimal). The OUTPUT goes active (low) immediately after the CLOCK transition resulting in terminal count, and it remains active for one clock period. The next CLOCK falling edge automatically transfers the content of the load register to the counter and returns the OUTPUT to the inactive (high) state.

2 GATE may be regarded as either an **output reset** or **synchronization** input signal in Mode 2. When low, the channel is enabled to down count. When high, the next CLOCK falling edge transfers the load register to the counter, restoring the preload value and synchronizing the output with the GATE input. Counting resumes when GATE goes low.

3 If OUTPUT is active when GATE goes high, the output is immediately forced to the inactive state regardless of CLOCK transitions. At the next CLOCK falling edge, the preload value is restored to the counter and counting resumes as soon as GATE is again low.

NOTE

In Mode 2, **preload value = 0000** is regarded as 10,000 (9999 + 1 decimal or FFFF + 1 hexadecimal). **Preload value = 0001** holds OUTPUT continuously inactive regardless of CLOCK or GATE activity.

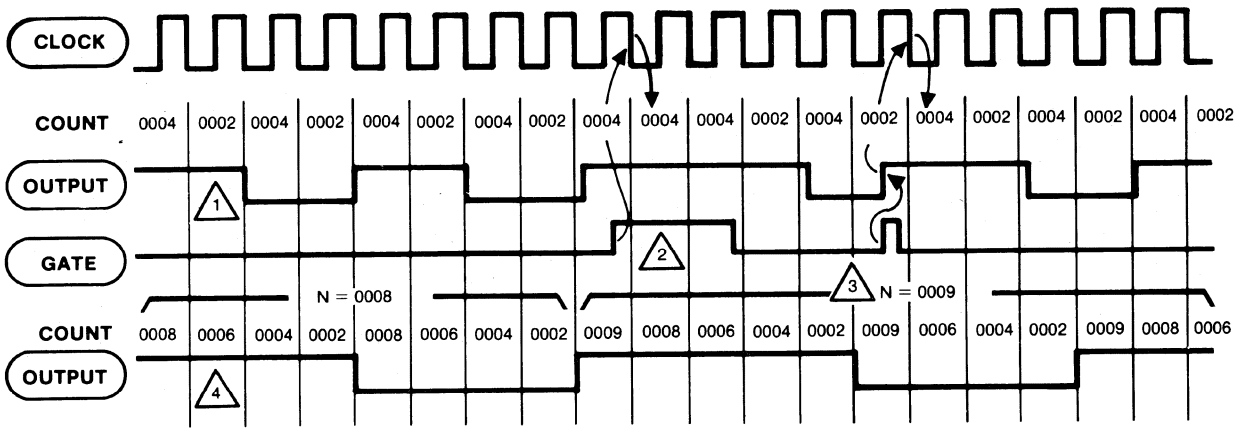


Figure 3-15. Counter/Timer Mode 3—Square Wave Generator (7804A)

NOTE

Due to internal comparison logic in the 8253-5 for Mode 3, certain initial values preloaded to the load register will cause unusual results:

0000 is regarded as 10,000 (9999 + 1 decimal, or FFFF + 1 hexadecimal).
0001 is regarded as 10,001 (9999 + 2 decimal, or FFFF + 2 hexadecimal).
0002 divides CLOCK by 2.
0003 produces a waveform that is inactive for one CLOCK period and active for 10,000 (9999 + 1 decimal, or FFFF + 1 hexadecimal) periods.

1 OUTPUT goes inactive (high) with the rising edge of WR* when Mode 3 is selected; counting stops regardless of CLOCK or GATE activity, and the count remaining from the previous mode (N) is frozen in the counter. In the lower three waveforms above, 0004 (decimal or hexadecimal) has been preloaded after the selection of Mode 3.

If GATE is high after the preload operation, the first CLOCK falling edge transfers the preload value from the load register to the counter and subsequent CLOCK falling edges decrement the counter toward terminal count.

Terminal count for Mode 3 is 0002 (decimal or hexadecimal); **unlike other modes**, the OUTPUT state change occurs at the CLOCK falling edge after the edge causing terminal count. When the OUTPUT changes state, the load register value is automatically restored to the counter and the process repeats, creating an OUTPUT square wave.

Note that, as long as the initial count value preloaded to the load register is an even number (bit 0 = 0), each CLOCK transition decrements the counter by 2.

2 GATE may be regarded as either an **output reset** or **synchronization** input signal in Mode 3. When low, the channel is enabled to down count. When high, the next CLOCK falling edge transfers the load register to the counter, restoring the preload value and synchronizing OUTPUT with the GATE input. Counting can resume when GATE is low.

3 If OUTPUT is active (low) when GATE goes high, OUTPUT is immediately forced inactive and the counter is reloaded from the load register.

4 The second OUTPUT waveform illustrates the difference between an even preload value and an odd value. The even value (0008 in the example) produces a symmetrical square wave output and causes every CLOCK falling edge to decrement the counter by two. The odd value (0009 in the example) produces an asymmetrical square wave with OUTPUT inactive (high) for one clock period longer than it is active (low). This is achieved by decrementing by **one** the first time, then by **two**, until the first terminal count; then by **three** the first time with OUTPUT active, followed by two until the second terminal count completes the OUTPUT waveform period.

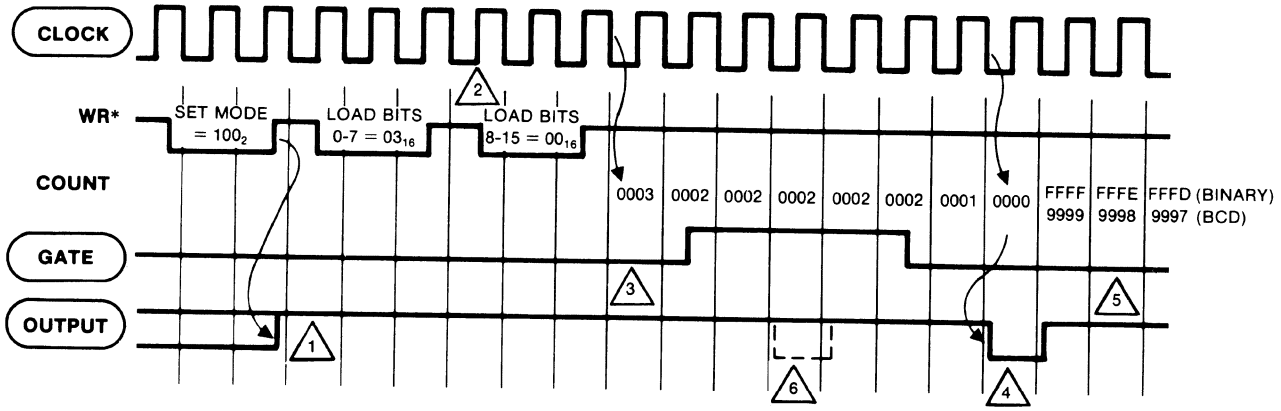


Figure 3-16. Counter/Timer Mode 4—Software-Triggered Strobe (7804A)

Mode 4 is identical to Mode 0, except that a single active pulse (strobe) is generated at terminal count. The "software trigger" is the preload operation.

1 OUTPUT goes inactive (high) with the rising edge of WR* when Mode 4 is selected; counting stops regardless of CLOCK or GATE activity, and the count remaining from the previous mode is frozen in the counter.

2 Counting cannot resume until one or two bytes of preload data (initial value) are written to the load register. The state of the mode control register's RL bits determines whether one byte or two are needed. CLOCK transitions occurring between write cycles are irrelevant until the channel is preloaded.

3 After the preload operation, the first CLOCK falling edge, with GATE active, transfers the preload value from the load register to the counter. Subsequent CLOCK edges decrement the count. GATE may be used to modulate the count if desired. Counting can only occur while GATE is active.

4 Terminal count for Mode 4 is 0000 (decimal or hexadecimal). Immediately after the CLOCK falling edge causing terminal count, OUTPUT goes active (low) and remains active until the next CLOCK falling edge. It then goes inactive (high) and remains inactive until a new mode is selected.

Thus the act of preloading the channel in Mode 4 acts as a trigger that initiates a time delay. After a delay of N CLOCK pulses, a strobe pulse is generated at OUTPUT.

5 After terminal count, the channel continues to decrement past 0000 according to the state of the BCD mode bit. The preload value is never reloaded to the counter. The only way to exit from Mode 4 is to write a new mode selection into the channel's mode control register.

6 The dotted pulse shows how OUTPUT would have responded if GATE had not gone inactive in the example.

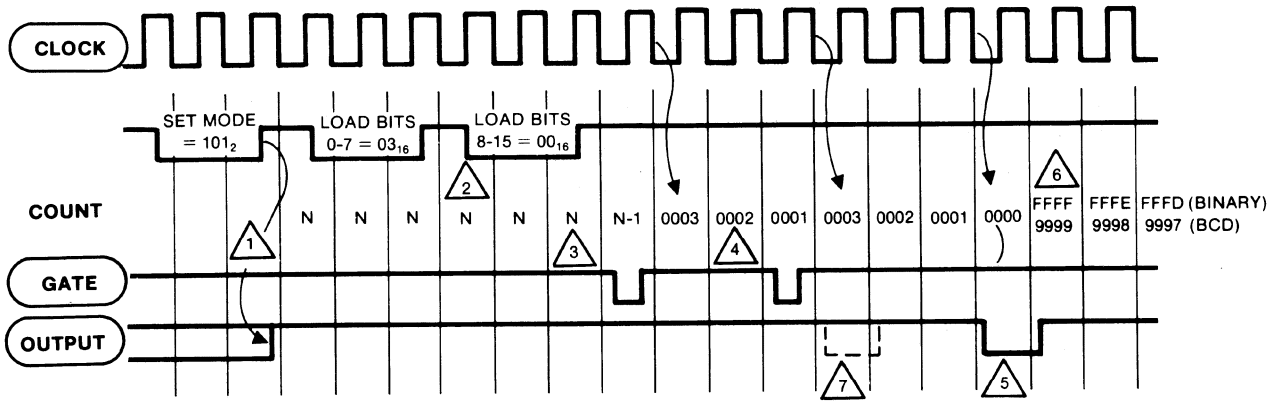


Figure 3-17. Counter/Timer Mode 5—Hardware-Triggered Strobe, Retriggerable (7804A)

Mode 5 is identical to Mode 1 except that a single active pulse (strobe) is generated at terminal count. The "hardware trigger" is the GATE falling edge.

1 OUTPUT goes inactive (high) with the rising edge of WR* when Mode 5 is selected; counting stops regardless of CLOCK or GATE activity, and the count remaining from the previous mode (N) is frozen in the counter.

CAUTION

Disable GATE by setting GTE = 0 in the program before selecting Mode 5. Do not reenable GATE until the preload value has been loaded. This prevents inadvertent OUTPUT activity.

2 Counting cannot resume until one or two bytes of preload data (initial value) are written to the load register. The state of the mode control register's RL bits determines whether one byte or two are needed. CLOCK transitions occurring between write cycles are irrelevant until the channel is preloaded.

3 GATE's edge triggers the delayed strobe. The next CLOCK falling edge, after the GATE edge, transfers the preload value from the load register into the counter; OUTPUT remains inactive (high). After triggering the count, GATE may remain high or low without affecting the count.

4 If another GATE edge occurs before terminal count, **retriggering** occurs. The preload value is again transferred from the load register to the counter on the next CLOCK falling edge, and down counting proceeds from the preload value. OUTPUT remains inactive without glitching.

5 Terminal count for Mode 5 is 0000. Immediately after the CLOCK edge causing terminal count, OUTPUT goes active (low) and remains low until the next CLOCK edge. It then goes inactive (high) and remains high until the next GATE trigger or until a new mode is selected.

Thus triggering the channel via GATE produces a delayed strobe pulse.

6 After terminal count, the channel continues to decrement past 0000 according to the state of the BCD mode bit. Decrementing continues freely until the next GATE trigger.

7 The dotted pulse shows how the OUTPUT would have responded if the GATE retrigger had not occurred in the example.

Interrupt

Each channel in the counter/timer has interrupts that can be individually enabled and disabled. The enabling and clearing of the interrupts are controlled by port F4. Figure 3-18 shows which bit corresponds to which channel. At power-up or reset, the interrupts are disabled. To enable an interrupt, a logic 1 should be written out to the correct bit.

When the interrupt is enabled for a particular channel and that channel's output goes low, an INTRQ* is generated. The interrupt is latched and can be read-in through the status port. See figure 3-19 for the bit assignments. If more than one channel has generated the interrupt, the status port must be read to determine which channel it was.

To clear the interrupt, a logic 1 must be written-out to the appropriate bit of the interrupt control port. The rising edge of the bit clears the interrupt. Therefore, if the bit is already set it must be cleared to a logic 0 and then set again to a logic 1.

Check the output waveform of the counter/timer mode. Keep in mind that the interrupt occurs when the output goes low. In some modes, use of the interrupt would be impractical. In Mode 0 for instance, the output goes low as soon as the mode is selected; however, even with this limitation virtually any application requiring interrupts can be accomplished with one of the six modes.

External Interrupts

The counter/timer can be used to input interrupt signals from interrupting devices. Use Mode 5 and preset the counter with a count of 1. The interrupting device should have its interrupt line tied to the gate signal of the appropriate channel. When the interrupting device sets its interrupt line low, the counter/timer generates an interrupt two time states later. Using the internal 2 MHz clock, the counter/timer interrupt occurs approximately 1 μs after the external device's interrupt.

BIT	FUNCTION
b7	Clear interrupt 2
b6	Clear interrupt 1
b5	Clear interrupt 0
b4	External control
b3	Enable interrupt 2
b2	Enable interrupt 1
b1	Enable interrupt 0
b0	Alternate address control

Figure 3-18. Interrupt Control Bit Assignments (7804A)

BIT	FUNCTION
b7	Input interrupt 2
b6	Input interrupt 1
b5	Input interrupt 0
b4	External status
b3	Unused
b2	Unused
b1	Unused
b0	Unused

Figure 3-19. Status Port Bit Assignments (7804A)

Cascaded Channel Delay

To extend the time delay available from one channel to two or three cascaded time delays, the output from one channel is used to trigger the gate of another channel. The number of counts and the channels required to perform the count are determined by the following formula:

$$N = \frac{\Delta T}{\tau}$$

Where N = number of counts required
ΔT = desired time delay
τ = 1/clock frequency

N equals a decimal number that must be converted into binary. Figure 3-20 shows the delay ranges for the single channel and cascaded channel.

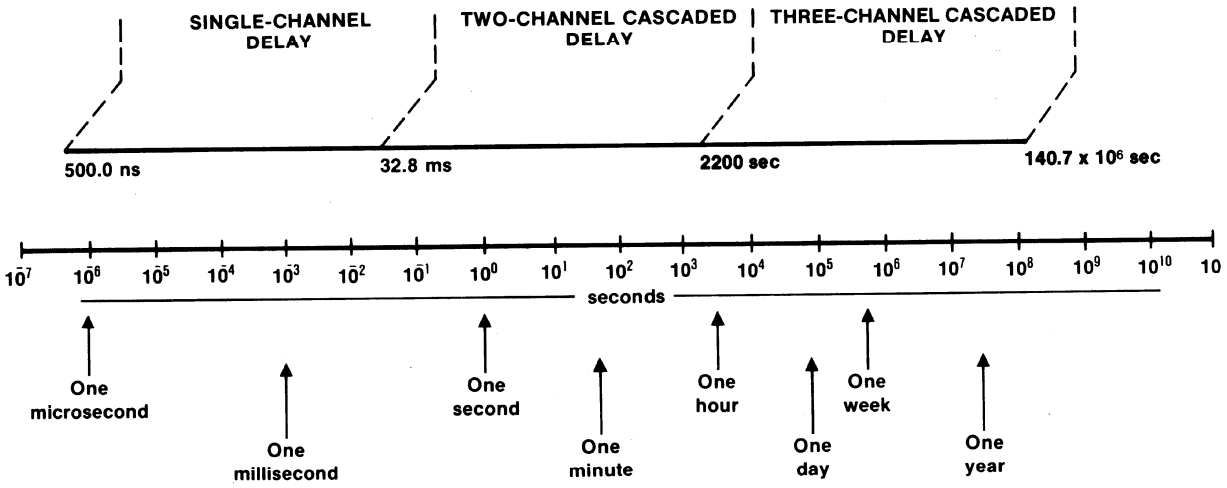


Figure 3-20. Single Channel and Cascaded Channel Delay Ranges (7804A)

SECTION 4
Operating Software

INTRODUCTION

This section contains hardware-level subroutine modules for operating the 7804A counter/timer card.

The software in this section can be used without license from Pro-Log. Although tested and believed to be correct, this software is not represented to be free from errors or copyright infringement, or appropriate for any particular application.

The subroutines are written in STD instruction mnemonics. The coding forms are grouped at the end of this section (figure 4-9). Individual subroutine specifications show memory requirements, entry requirements, and exit characteristics for each path in the program. Timing and other necessary information are also provided.

MEMORY ADDRESSES

Full memory addreses are shown in the subroutine documentation. They are the preferred addresses to allow the subroutines to work with those provided for other Series 7000 STD BUS cards from Pro-Log. The program addresses correspond to 7804A onboard memory sockets as shipped.

If your system cannot use the memory addresses in the 7804A software package, simply change the memory page addresses as required when loading these modules into your system. Memory addresses that **must** be located in RAM are noted on the program coding forms. Other memory addresses shown are intended to be ROM locations, but may also be RAM locations.

I/O PORT ADDRESSES

The 7804A I/O ports are assigned preferred addresses F0-F5 for compatibility with other Series 7000 cards. Section 2 shows how to remap these addresses if necessary. This software can be used by changing the port addresses when loading the subroutines into your system.

SUBROUTINE FUNCTIONS

Two subroutines are provided in this section. The first provides a time delay, variable in increments of 1 ms. The second is an interrupt service routine, designed to determine which channel generated the interrupt and to direct the processor to the correct service routine.

The locations of the subroutine in memory, and the RAM and stack areas they use are shown in figures 4-1 and 4-2.

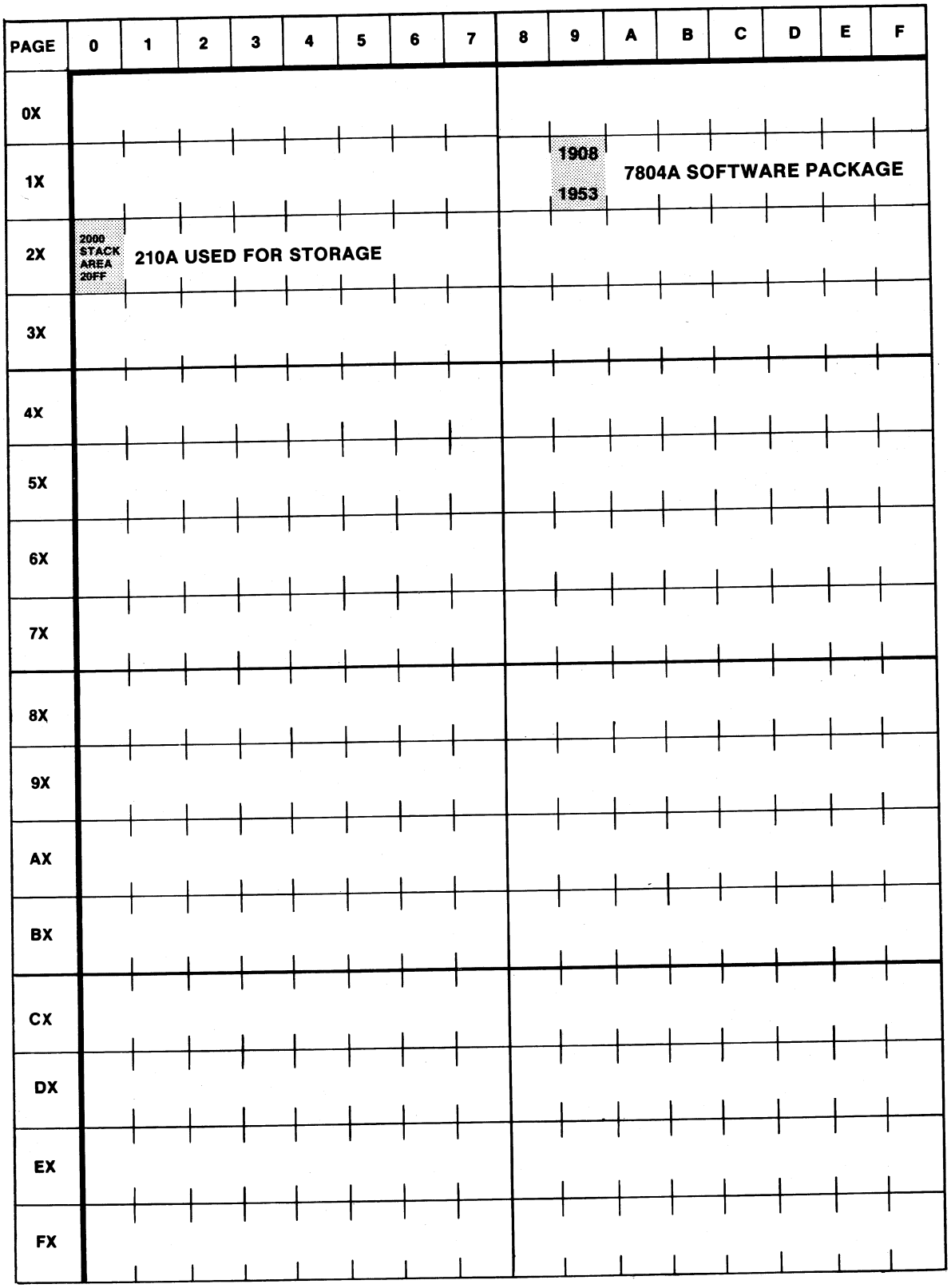


Figure 4-1. 64K Address Map for Software Package (7804A)

PAGE ADDRESS 19

LINE	LABEL
00	(VAR Δ)
01	
02	
03	
04	
05	
06	
07	
08	
09	
0A	
0B	
0C	
0D	
0E	
0F	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
1A	
1B	
1C	
1D	
1E	
1F	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
2A	
2B	
2C	
2D	
2E	
2F	
30	(INTR CHECK)
31	
32	
33	
34	
35	
36	
37	
38	
39	
3A	
3B	
3C	
3D	
3E	
3F	

LINE	LABEL
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
4A	
4B	
4C	
4D	
4E	
4F	
50	
51	
52	
53	
54	
55	
56	
57	
58	
59	
5A	
5B	
5C	
5D	
5E	
5F	
60	
61	
62	
63	
64	
65	
66	
67	
68	
69	
6A	
6B	
6C	
6D	
6E	
6F	
70	
71	
72	
73	
74	
75	
76	
77	
78	
79	
7A	
7B	
7C	
7D	
7E	
7F	

LINE	LABEL
80	
81	
82	
83	
84	
85	
86	
87	
88	
89	
8A	
8B	
8C	
8D	
8E	
8F	
90	
91	
92	
93	
94	
95	
96	
97	
98	
99	
9A	
9B	
9C	
9D	
9E	
9F	
A0	
A1	
A2	
A3	
A4	
A5	
A6	
A7	
A8	
A9	
AA	
AB	
AC	
AD	
AE	
AF	
B0	
B1	
B2	
B3	
B4	
B5	
B6	
B7	
B8	
B9	
BA	
BB	
BC	
BD	
BE	
BF	

LINE	LABEL
C0	
C1	
C2	
C3	
C4	
C5	
C6	
C7	
C8	
C9	
CA	
CB	
CC	
CD	
CE	
CF	
D0	
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	
D9	
DA	
DB	
DC	
DD	
DE	
DF	
E0	
E1	
E2	
E3	
E4	
E5	
E6	
E7	
E8	
E9	
EA	
EB	
EC	
ED	
EE	
EF	
F0	
F1	
F2	
F3	
F4	
F5	
F6	
F7	
F8	
F9	
FA	
FB	
FC	
FD	
FE	
FF	

Figure 4-2. Page Address Map for Software Package (7804A)

SUBROUTINE (VAR Δ)

Start Address: 1900

This is a variable delay subroutine. It is variable in increments of 1ms. It is entered with the number of milliseconds you wish the delay to last, in the B & C register pair, in hexadecimal. At the end of the delay an interrupt is generated. Counter/timer channels 1 and 2 are used; channel 1 generates the interrupt.

The output of channel 2 (pin 8) on the J1 connector must be connected to the gate of channel 1 (pin 10). The external control line (pin 2) must be tied to the gate of channel 2 (pin 4), using the shorting connectors provided with the 7804A card.

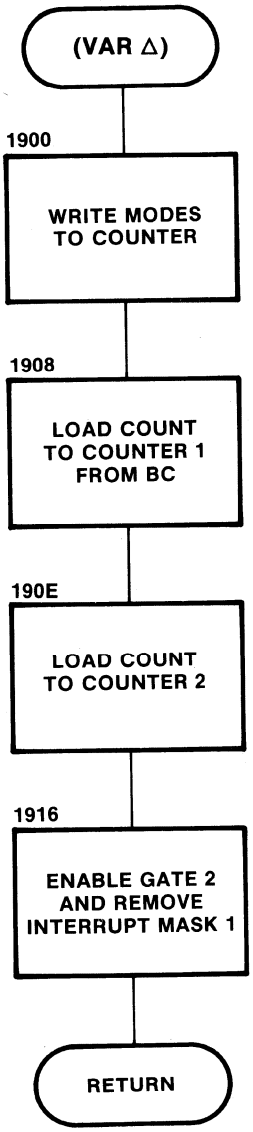


Figure 4-3. Flowchart—Subroutine (VAR Δ) (7804A)

RAM address 210A is used for storing the current state of output port F4. Port F4 enables and clears interrupts, external control, and alternate address control. Address 210A must be cleared by the user's program before the port is used. Thereafter it should be loaded with whatever is written to the port whenever the port is used.

Subroutine (VAR Δ) does not initialize the Z80A's interrupt mode, nor does it enable the INTRQ* line. The user's program has control over these functions.

The registers and RAM memory affected by (VAR Δ) are shown in figure 4-4. The total memory used and the execution time are shown in figure 4-5.

PARAMETER		ENTRY REQUIREMENTS	EXIT CONDITION	COMMENT
ELEMENT	ADDRESS			
Register Pair	BC	No. of ms	Unchanged	
Register	A	XX	??	
Register	F	XX	??	
RAM Memory	210A	Current Status of Port F4	Current Status of Port F4	External Control = 1 Channel 1 Interrupt Enabled

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-4. Register and Memory Allocation Subroutine (VAR Δ) (7804A)

SYMBOL	SUBROUTINE PARAMETER	LIMITS		UNITS
		MIN	MAX	
Ns	Stack Memory		0	Bytes
Np	Program Memory		33	Bytes
Npt	Total Program Memory		33	Bytes
Nr	RAM Memory		1	Bytes
Ne	Execution Time		156	Time States

Figure 4-5. Characteristics of Subroutine (VAR Δ)(7804A)

SUBROUTINE (INTR CHECK)

Start Address: 1930

This subroutine aids in the use of interrupts generated by the counter/timer. The processor must be initialized by selecting interrupt mode 1 and enabling the Z80A's INTRQ* line.

When an interrupt occurs, the processor jumps to address 0038. At this address, you must supply a program that does one of two things. If the counter/timer is the only source of interrupt, your program should simply jump to address 1930, which is where the subroutine resides. If there are other devices in the system that can generate an interrupt, your program should first determine if they were the source of this interrupt. If they were not, you can assume that the counter/timer generated the interrupt. At this point, your program should jump to address 1930. Subroutine (INTR CHECK) reads and stores the interrupt latches. It then clears any counter/timer interrupt that is latched and determines which channel generated the interrupt.

The processor jumps to your interrupt service routine, for which there are three jump-to-subroutine instructions, one for each channel. The addresses that these instructions jump to have been left blank. You must provide these addresses and the service routines for each channel.

When an interrupt occurs, the Z80A's INTRQ* line is disabled. The line is reenabled after your counter/timer interrupt service routine has been completed. Any INTRQ* that has occurred during the interrupt service will be acknowledged when INTRQ* is reenabled.

The register and RAM requirements are shown in figure 4-7. As with the (VAR Δ) subroutine, RAM address 210A is used to keep track of what has been output to port F4. The total memory and execution time are shown in figure 4-8.

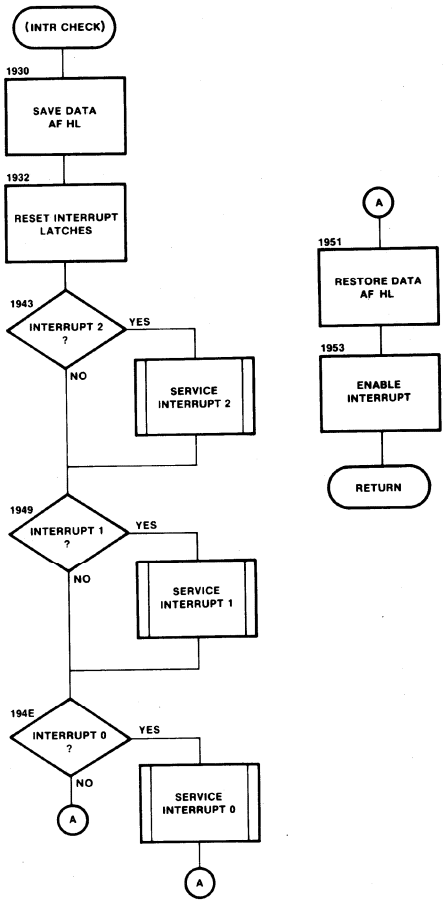


Figure 4-6. Flowchart—Subroutine (INTR CHECK) (7804A)

PARAMETER		ENTRY REQUIREMENTS	EXIT CONDITION	COMMENT
ELEMENT	ADDRESS			
RAM Memory	210A	Current Status of Port F4	Unchanged	

Figure 4-7. Register and Memory Allocation Subroutine (INTR CHECK) (7804A)

SYMBOL	SUBROUTINE PARAMETER	LIMITS		UNITS
		MIN	MAX	
Ns	Stack Memory		8	Bytes
Np	Program Memory		37	Bytes
Npt	Total Program Memory		37	Bytes
Nr	RAM Memory		1	Bytes
Ne	Execution Time		242	Time States

Figure 4-8. Characteristics of Subroutine (INTR CHECK) (7804A)

CODING FORMS

HEXADECIMAL			MNEMONIC			TITLE VARIABLE Δ DATE 2-1-84
PAGE ADR	LINE ADR	INSTR.	LABEL	INSTR.	MODIFIER	COMMENTS
19	00	3E	(VAR Δ)	I DAT		WRITE MODE TO COUNTER : CHANNEL 1
	1	78		—	0111 1000	MODE 4, HEX
	2	D3		OPA		
	3	F3		—	F3	
	4	3F		LDA I		WRITE MODE TO COUNTER: CHANNEL 2
	5	B5		—	1011 0101	MODE 2, DECIMAL COUNT
	6	D3		OPA		
	7	F3		—	F3	
	8	79		LDA	C	LOAD COUNT (NUMBER OF MILLISECONDS)
	9	D3		OPA		TO COUNTER 1
	A	F1		—	F1	
	B	78		LDA	B	
	C	D3		OPA		
	D	F1		—	F1	
	E	3E		LDAI		LOAD COUNT (1MSEC) TO COUNTER 2
	F	00		—	00	
	10	D3		OPA		
	1	F2		—	F2	
	2	3E		LDAI		
	3	2D		—	2D	
	4	D3		OPA		
	5	F2		—	F2	
	6	3A		LDAD		SET GATE OF COUNTER 1 HIGH, ENABLE
	7	0A		—	210A	INTA 1 MASK WITHOUT DISTURBING DATA
	8	21		—		PREVIOUSLY LATCHED AT OUTPUT PORT
	9	F6		ORAI		
	A	14		—	14	
	B	32		STAD		
	C	0A		—	210A	
	D	21		—		
	E	D3		OPA		
	F	F4		—	F4	
19	20	C9		RTS		

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE INTERRUPT CHECK — DATE 2-1-84

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
19	30	F5	(INTRA CHECK)	PSP	AF	SAVE DATA IN AF HL
	1	E5		PSP	HL	
	2	21		LDPI	HL	CLEAR INTERRUPT LATCHES THAT ARE SET
	3	OA		—		WITHOUT DISTURBING DATA LATCHED AT
	4	21		—		OUTPUT PORT F4. SAVE STATUS PORT
	5	DB		IPA		INFO IN STACK.
	6	F4		—	F4	
	7	F5		PSP	AF	
	8	E6		ANA I		
	9	EO		—	EO	
	A	B6		ORAN	HL	
	B	D3		OPA		
	C	F4		—	F4	
	D	7E		LDAN	HL	
	E	D3		OPA		
	F	F4		—	F4	
	40	F1		PLP	AF	RETRIEVE STATUS PORT INFO. SERVICE INTR
	1	17		RLAC		IF INTR 2 LATCH IS SET
	2	F5		PSP	AF	
	3	DC		JS	C1	
	4			—	(SERVICE INT 2)	
	5			—		
	6	F1		PLP	AF	RETRIEVE STATUS PORT INFO. SERVICE
	7	17		RLAC		INTR B IF INTR 1 LATCH IS SET
	8	F5		PSP	AF	
	9	DC		JS	C1	
	A			—	(SERVICE INT 1)	
	B			—		
	C	F1		PLP	AF	RETRIEVE STATUS PORT INFO. SERVICE
	D	17		RLAC		INTR IF INTR O LATCH IS SET
	E	DC		JS	C1	
	F			—	(SERVICE INT O)	
19	50			—		
	1	E1		PLP	HL	RESTORE DATA IN REGISTERS
	2	F1		PLP	AF	
	3	FB		ENI		ENABLE INTERRUPT AND RETURN
	4	C9		RTS		
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

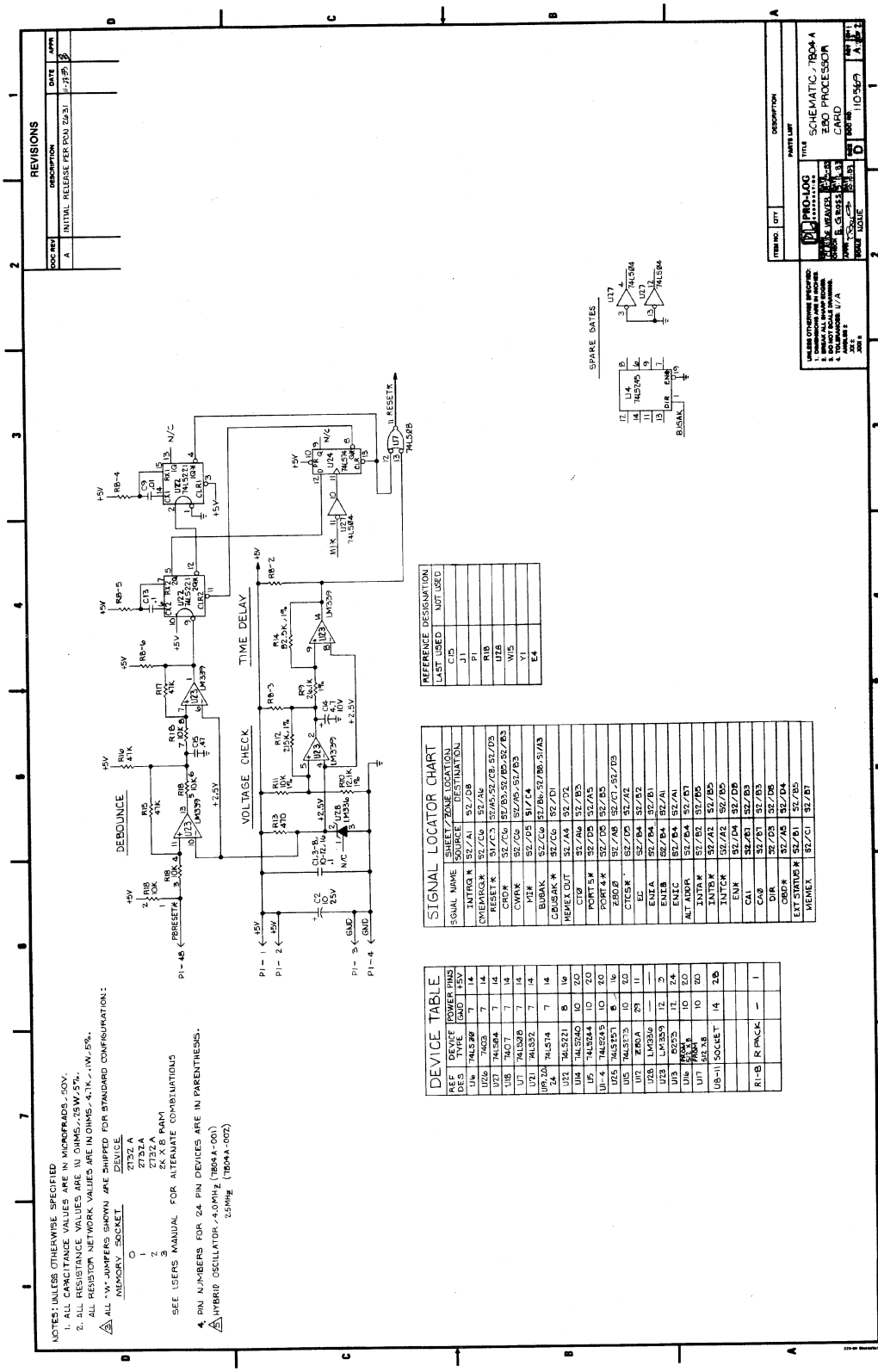
100001 2/77

SECTION 5
Maintenance

REFERENCE DRAWINGS

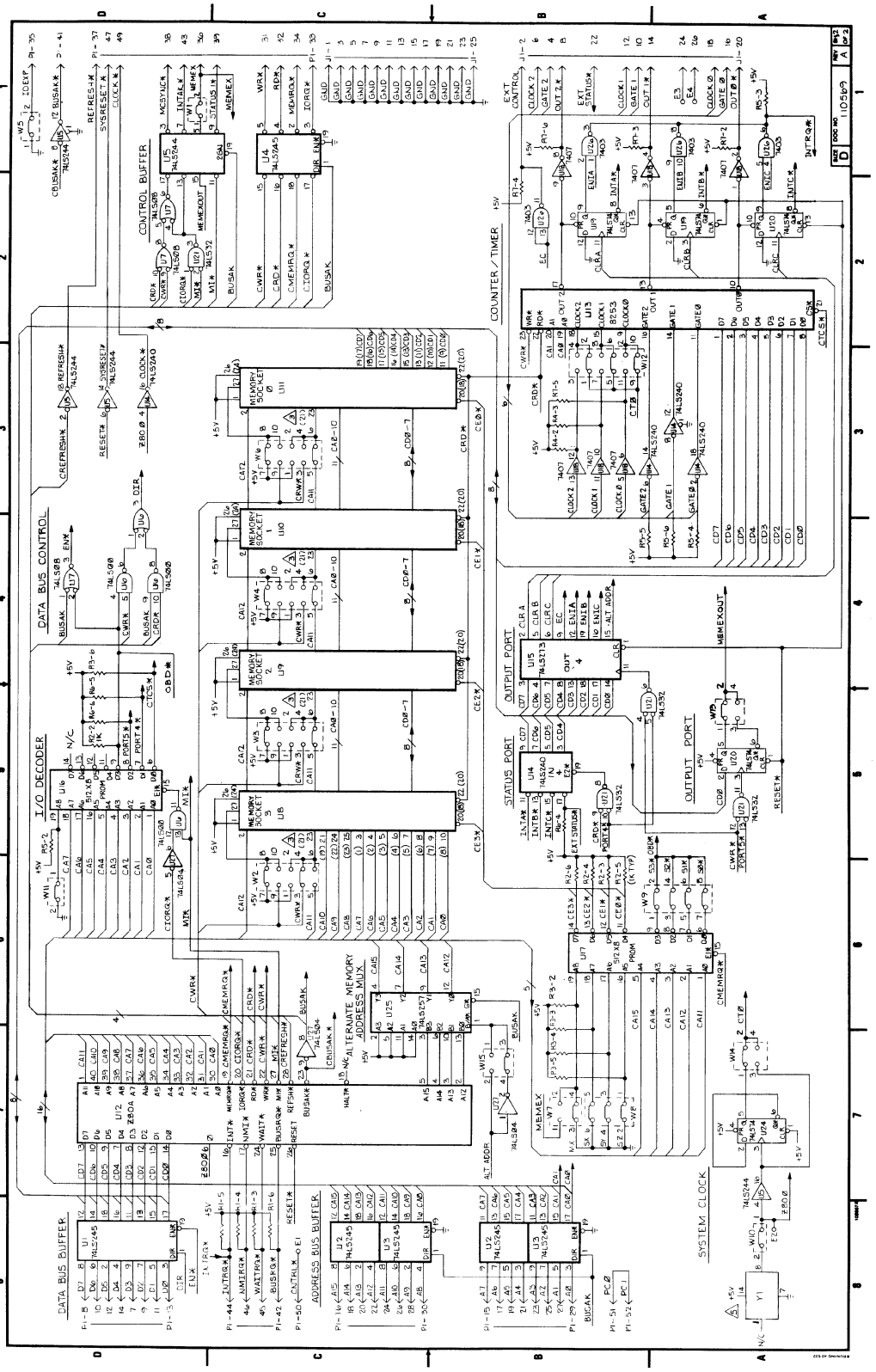
The schematic (figure 5-1) and assembly drawing (figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. Because improvements to the product may have been made since this manual was published, they may differ in some respects from the card and documentation that the user receives from Pro-Log.

The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.


REVISIONS
DESCRIPTION
INITIAL RELEASE PER PCN 22/31
SCHEMATIC, 7804A Z80 PROCESSOR CARD
PRO-LOG
DEBOUNCE
VOLTAGE CHECK
TIME DELAY
SPARE GATES
SIGNAL LOCATOR CHART
DEVICE TABLE
REFERENCE DESIGNATION
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITANCE VALUES ARE IN MICROFRADS, 50V.
2. ALL RESISTANCE VALUES ARE IN OHMS, .25W, 5%.
ALL RESISTOR NETWORK VALUES ARE IN OHMS, 4.7K, 1W, 5%.
ALL "W" JUMPERS SHOWN ARE SHIPPED FOR STANDARD CONFIGURATION:
MEMORY SOCKET DEVICE
0 2732 A
1 2732 A
2 2K X 8 RAM
3
SEE USERS MANUAL FOR ALTERNATE COMBINATIONS
4. PIN NUMBERS FOR 24 PIN DEVICES ARE IN PARENTHESIS.
HYBRID OSCILLATOR, 4.0MHz (7804A-001)
2.5MHz (7804A-002)

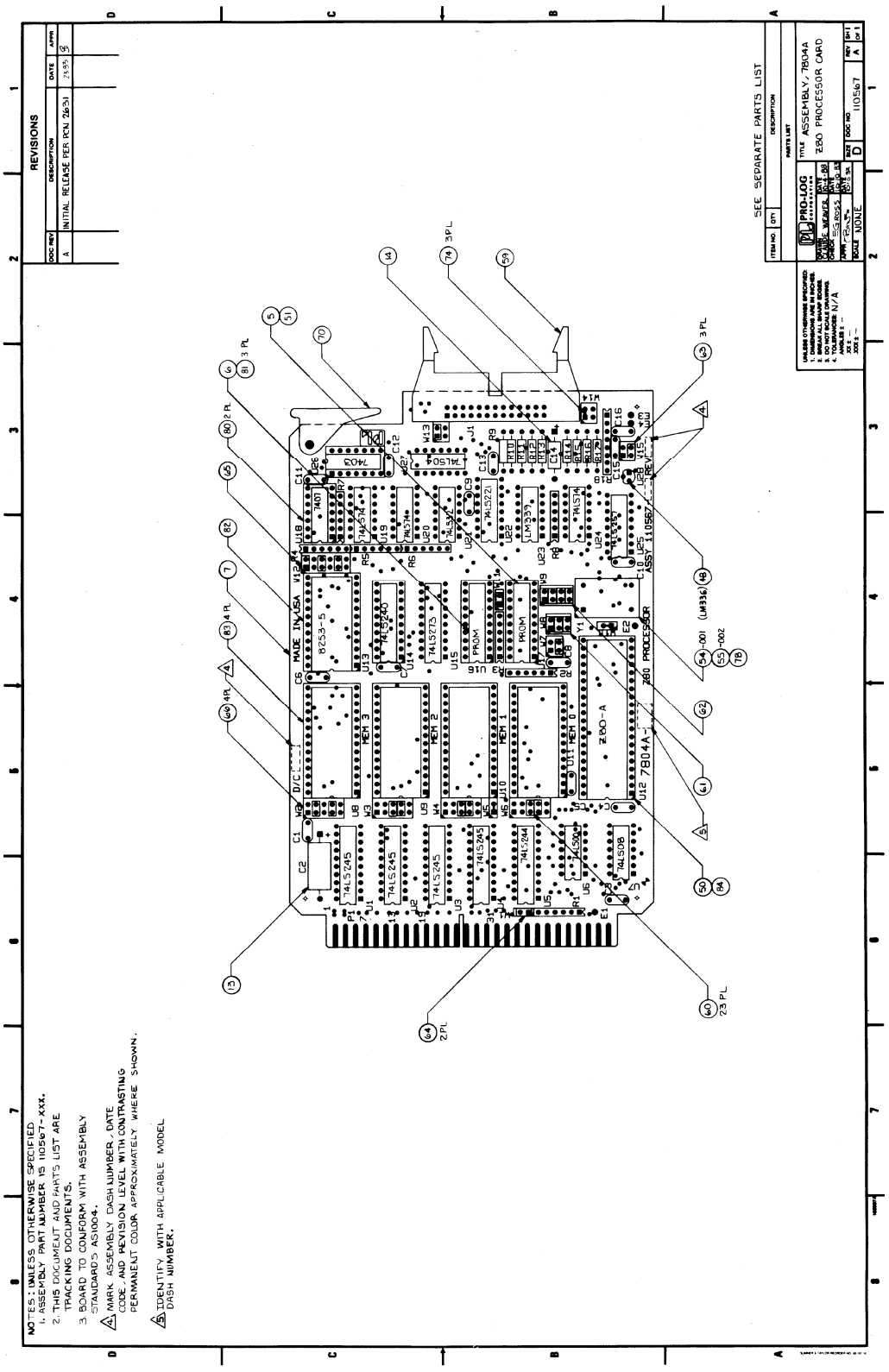
(Reference only. See documents shipped with the card.)

Figure 5-1. Schematic Page 1 (7804A)



(Reference only. See documents shipped with the card.)

Figure 5-2. Schematic Page 2 (7804A)



(Reference only. See documents shipped with the card)

Figure 5-2. Assembly Drawing (7804A)

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call Customer Support at (800) 538-9570, ext. 3617. In California call (408) 646-3617 from 7 a.m. to 3 p.m. (PST).
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

CAUTION

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO #_____.

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned f.o.b. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.